A10 Transport Stream Controller

1. Overview

The transport stream controller is responsible for de-multiplexing and pre-processing the input multimedia data defined in ISO/IEC 13818-1.

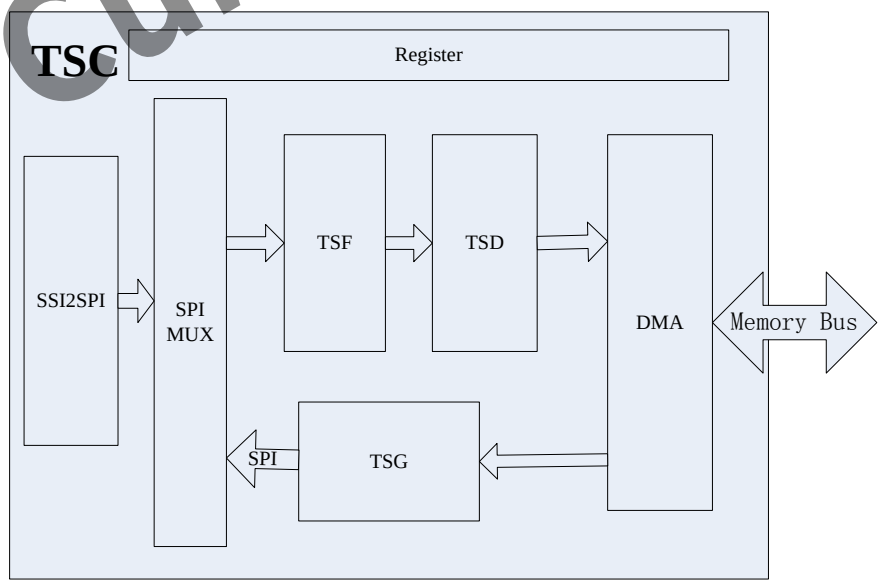
The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before Packets are stored to memory by DMA, it can be pre-processed by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multi-media application cases, for example: DVB STB, IPTV, Streaming-media Box, multi-media players and so on.

The Transport Stream Controller (TSC) features:

- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detection
- Configurable SPI transport stream generator for streams in DRAM memory
- DMA is supported for data transfer
- Support DVB-CSA V1.1 Descrambler

The Top Diagram of TSC is shown below:



TSC: TS Controler TSG: TS Generator

TSD: TS Descrambler TSF: TS Filter

Figure1 TSC Diagram

2. Related Registers

2.1. TSC Control Registers

Offset: 0x00			Register Name: TSC_CTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/
1	R/W	0	TSCSR TSC Soft Reset An software writting '1' will initiate a reset to all logic of TSC. And this bit will be cleared automaticly after reset.
0	R/W	0	TSCEn TSC Enable 0 – Disable 1 – Enable

2.2. TSC Status Register

Offset: 0x04			Register Name: TSC_STAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

2.3. TSC Port Control Register

Offset: 0x10			Register Name: TSC_PCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16	R/W	0	TSOutPort0Ctrl TS Output Port0 Control 0 – SPI 1 – SSI
15:2	/	/	/
1	R/W	0	TSInPort1Ctrl TS Input Port1 Control 0 – SPI 1 – SSI
0	R/W	0	TSInPort0Ctrl

			TS Input Port0 Control 0 – SPI 1 – SSI

2.4. TSC Port Parameter Register

Offset: 0x14			Register Name: TSC_PPARR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0x00	TSOutPort0Par TS Output Port0 Parameters Bit / Definition 7:5 / / 4 / SSI data order 0: MSB first for one byte data 1: LSB first for one byte data 3 / CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing 2 / ERROR signal polarity 0: High level active 1: Low level active 1 / DVALID signal polarity 0: High level active 1: Low level active 0 / PSYNC signal polarity 0: High level active 1: Low level active
23:16	/	/	/
15:8	R/W	0x00	TSInPort1Par TS Input Port1 Parameters **Bit** / **Definition** 7:5 / Reserved 4 / SSI data order 0: MSB first for one byte data 1: LSB first for one byte data 3 / CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing

			2 ERROR signal polarity 0: High level active 1: Low level active 1 DVALID signal polarity 0: High level active 1: Low level active 0 PSYNC signal polarity 0: High level active 1: Low level active
7:0	R/W	0x00	TSInPort0Par TS Input Port0 Parameters **Bit** / **Definition** 7:5 Reserved 4 SSI data order 0: MSB first for one byte data 1: LSB first for one byte data 3 CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing 2 ERROR signal polarity 0: High level active 1: Low level active 1 DVALID signal polarity 0: High level active 1: Low level active 0 PSYNC signal polarity 0: High level active 1: Low level active

2.5. TSC TSF Input Multiplex Control Register

Offset: 0x20			**Register Name: TSC_TSFMUXR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:4	R/W	0x0	TSF1InputMuxCtrl TSF1 Input Multiplex Control 0x0 –Data from TSG 0x1 –Data from TS IN Port0

			0x2 –Data from TS IN Port1 Others – Reserved
3:0	R/W	0x0	TSF0InputMuxCtrl TSF0 Input Multiplex Control 0x0 –Data from TSG 0x1 –Data from TS IN Port0 0x2 –Data from TS IN Port1 Others – Reserved

2.6. TSC Port Output Multiplex Control Register

Offset: 0x28			**Register Name: TSC_TSFMUXR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
3:0	R/W	0x0	TSPortOutputMuxCtrl TS Port Output Multiplex Control 0x0 – Data from TSG 0x1 –Data from TS IN Port0 0x2 –Data from TS IN Port1 Others – Reserved

2.7. TSG Control and Status Register

Offset: TSG+0x00			**Register Name: TSG_CSR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:24	R	0	TSGSts Status for TS Generator 0: IDLE state 1: Running state 2: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0	TSGLBufMode Loop Buffer Mode When set to ‘1’, the TSG external buffer is in loop mode.
8	R/W	0	TSGSyncByteChkEn Sync Byte Check Enable

			Enable/ Disable check SYNC byte fro receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enable, the interrupt would happen.
7:3	/	/	/
2	R/W	0	TSGPauseBit Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0	TSGStopBit Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0	TSGStartBit Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

2.8. TSG Packet Parameter Register

Offset: TSG+0x04			**Register Name: TSG_PPR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position

			Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

2.9. TSG Interrupt Enable and Status Register

Offset: TSG+0x08			Register Name: TSG_IESR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R/W	0	TSGEndIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0	TSGErrSyncByteIE TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TSGEndSts TS Generator (TSG) End Status Write ‘1’ to clear.
2	R/W	0	TSGFFSts TS Generator (TSG) Full Finish Status Write ‘1’ to clear.

1	R/W	0	TSGHFSts TS Generator (TSG) Half Finish Status Write '1' to clear.
0	R/W	0	TSGErrSyncByteSts TS Generator (TSG) Error Sync Byte Status Write '1' to clear.

2.10. TSG Clock Control Register

Offset: TSG+0x0c			Register Name: TSG_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(16*(D+1)). Fi is the input special clock of TSC, and D must not be less than N.

2.11. TSG Buffer Base Address Register

Offset: TSG+0x10			Register Name: TSG_BBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	RW	0x0	TSGBufBase Buffer Base Address This value is a start address of TSG buffer. Note: This value should be 4-word (16Bytes) align, and the lowest 4-bit of this value should be zero.

2.12. TSG Buffer Size Register

Offset: TSG+0x14	Register Name: TSG_BSZR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:24	/	/	/
23:0	R/W	0	TSGBufSize Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16Bytes) align, and the lowest 4 bits should be zero.

2.13. TSG Buffer Pointer Register

Offset: TSG+0x18			Register Name: TSG_BPR Default Value: 0x1fff_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R	0	TSGBufPtr Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

2.14. TSF Control and Status Register

Offset: TSF+0x00			Register Name: TSF_CSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:1	/	/	/
0			TSFGSR TSF Global Soft Reset An software writing '1' will reset all status and state machine of TSF. And it's cleared by hardware after reset. An software writing '0' has no effect.

2.15. TSF Packet Parameter Register

Offset: TSF+0x04			Register Name: TSF_PPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	R/W	0	LostSyncThd Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0	SyncThd

			Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0	SyncMthd Packet Sync Method 0: By PSYNC signal 1: By sync byte 2: By both PSYNC and Sync Byte 3: Reserved
7	R/W	0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

2.16. TSF Interrupt Enable and Status Register

Offset: TSF+0x08			**Register Name: TSF_IESR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R/W	0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable

17	R/W	0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write '1' to clear.
2	R/W	0	TSFPPDIS TS PCR Packet Found Status When it is '1', one TS PCR Packet is found. Write '1' to clear.
1	R	0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 16 channels. It would be cleared to zero after all channels status bits are cleared.
0	R	0	TSFCDIS TS PID Filter (TSF) Channel DMA status It is global status for 16 channels. It would be cleared to zero after all channels status bits are cleared.

2.17. TSF DMA Interrupt Enable Register

Offset: TSF+0x10			**Register Name: TSF_DIER** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

2.18. TSF Overlap Interrupt Enable Register

Offset: TSF+0x14			**Register Name: TSF_OIER** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**

31:0	R/W	0x0	OLPIE Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

2.19. TSF DMA Interrupt Status Register

Offset: TSF+0x18			Register Name: TSF_DISR Default Value: 0x3FFF_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMAIS DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

2.20. TSF Overlap Interrupt Status Register

Offset: TSF+0x1c			Register Name: TSF_OISR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	OLPIS Overlap Interrupt Status Overlap interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

2.21. TSF PCR Control Register

Offset: TSF+0x20			Register Name: TSF_PCRCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16	R/W	0	PCRDE PCR Detecting Enable 0: Disable 1: Enable

15:13	/	/	/
12:8	R/W	0	PCRCIND Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0	PCRLSB PCR Contest LSB 1 bit PCR[0]

2.22. TSF PCR Data Register

Offset: TSF+0x24			Register Name: TSF_PCRDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	PCRMSB PCR Data High 32 bits PCR[33:1]

2.23. TSF Channel Enable Register

Offset: TSF+0x30			Register Name: TSF_CENR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	FilterEn Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

2.24. TSF Channel PES Enable Register

Offset: TSF+0x34			Register Name: TSF_CPER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	PESEn PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during corresponding channel enable.

2.25. TSF Channel Descramble Enable Register

Offset: TSF+0x38			Register Name: TSF_CDER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DescEn Descramble Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

2.26. TSF Channel Index Register

Offset: TSF+0x3c			Register Name: TSF_CINDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

2.27. TSF Channel Control Register

Offset: TSF+0x40			Register Name: TSF_CCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

2.28. TSF Channel Status Register

Offset: TSF+0x44			Register Name: TSF_CSTAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

2.29. TSF Channel CW Index Register

Offset: TSF+0x48			Register Name: TSF_CCWIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is '0'.

2.30. TSF Channel PID Register

Offset: TSF+0x4c			Register Name: TSF_CPIDR Default Value: 0x1fff_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x1fff	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

2.31. TSF Channel Buffer Base Address Register

Offset: TSF+0x50			Register Name: TSF_CBBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	TSFBufBAddr Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

2.32. TSF Channel Buffer Size Register

Offset: TSF+0x54	Register Name: TSF_CBSZR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:26	/	/	/
25:24	R/W	0	CHDMAIntThd DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 0: 1/2 data buffer packet size 1: 1/4 data buffer packet size 2: 1/8 data buffer packet size 3: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0	CHBufPktSz Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16Bytes) aligned. The LSB four bits should be zero.

2.33. TSF Channel Buffer Write Pointer Register

Offset: TSF+0x58			Register Name: TSF_CBWPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:0	R/W	0	BufWrPtr Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by software when the corresponding channel is enable.

2.34. TSF Channel Buffer Read Pointer Register

Offset: TSF+0x5c			Register Name: TSF_CBRPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

31:21	/	/	/
20:0	R/W	0	BufRdPtr Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

2.35. TSD Control Register

Offset: TSD+0x00			Register Name: TSD_CTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	
1:0	R/W	0x0	DescArith Descramble Arithmetic 00: DVB CSA V1.1 Others: Reserved

2.36. TSD Status Register

Offset: TSD+0x04			Register Name: TSD_STAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

2.37. TSD Control Word Index Register

Offset: TSD+0x1c			Register Name: TSD_CWIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the Control index for Control word access. Range is from 0x00 to 0x7.
3:2	/	/	/
1:0	R/W	0x0	CWII Control Word Internal Index 0 – Odd Control Word Low 32-bit, OCW[31:0]; 1 – Odd Control Word High 32-bit, OCW[63:32]; 2 – Even Control Word Low 32-bit, ECW[31:0]; 3 – Even Control Word High 32-bit, ECW[63:0];

2.38. TSD Control Word Register

Offset: TSD+0x20			Register Name: TSD_CWR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	CWD Content of Control Word corresponding to the TSD_CWIR value

3. TS Clock Requirement

Clock Name	Description	Requirement
HCLK	AHB bus clock	
TS_CLK	Clock of TS Stream in SPI mode	
TSC_CLK	TS serial clock from CCU	TSC_CLK >=16*TS_CLK

4. Declaration

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