

AllwinnerA83T Datasheet

Octa-Core Tablet Processor

Revision 1.1

Sep. 23, 2014

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REVISION HISTORY

| Version | Date | Description |
|---------|-------------|--------------------------------|
| 1.0 | Aug.25,2014 | Initial release version |
| 1.1 | Sep.23,2014 | Correct Pin/Signal Description |

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1. OVERVIEW

The Allwinner's A83T is a remarkably lower power, high performance octa-core mobile application processor based on ARM Cortex™-A7 CPU along with SGX544MP1 GPU architecture. It is also highly competitive in term of system cost thanks to its high system integration and is capable of delivering excellent user experience while maintaining low power consumption.

Main features of A83T include:

- CPU architecture: Based on an octa-core Cortex™-A7 CPU architecture, the most power efficient CPU core ARM's ever developed.
- Graphics: A83T adopts the extensively implemented and technically mature PowerVR SGX544MP1 to provide mobile users with superior experience in web browsing, video playback and games; OpenGL ES1.1/2.0, OpenCL1.1 and DirectX 9.3 standards are supported.
- Video Engine: Multi-format playback of up to 1080P high-definition video, and support MPEG1/2, MPEG4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP8, WMV9/VC1, JPEG/MJPEG standards with dedicated hardware, and HEVC/H.265 decoder 1080p@30fps with software.
- Display: Supports RGB/LVDS/DSI/HDMI/CVBS interface to 1920x1200 resolution. Four-lane MIPI DSI is integrated as well.
- Memory Controller: Support LPDDR2/LPDDR3/DDR3 /DDR3L SDRAM, NAND Flash, Nor-Flash, SD/eMMC.
- HawkView™ ISP: Support camera up to 8MPixels@30fps, better spatial de-noise and chrominance de-noise, Zone-based AE/AF/AWB statistics, Programmable color correction, Anti-flick detection statistics.

To reduce total system cost and enhance overall functionality, in addition to these major elements, A83T has a broad range of hardware peripherals such as MIPI CSI, LCD controller, Power management, DMA, Timers, High Speed Timer, Security System, GPIO, Digital Audio, UART, SPI, I2C, USB2.0, TWI etc.

A83T application usage is extremely diverse on tablets and smartphones: users listen to music, watch movies, browse the web, share photos, play games, send emails, and more. When combined with Allwinner's PMIC chip that supports CoolFlex™ technology, A83T enables devices to run different applications more efficiently on different CPU cores, which build a range of low-power devices and a better user experience.

2. FEATURE

2.1. CPU Architecture

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4
- Support LPAE
- 32KB I-cache and 32KB D-cache per CPU
- 1MB L2-cache

2.2. GPU Architecture

- PowerVR SGX544MP1
- Support OpenGL ES 1.1/2.0
- Support OpenCL 1.1
- Support Directx 9.3 standards
- Support RenderScript

2.3. Memory Subsystem

Boot ROM

- On-chip ROM boot loader
- Size:96KB
- Support secure boot and non-secure boot
- Support system boot from Raw NAND, eMMC, SD/TF card and SPI Nor Flash
- Support system code download through USB DRD(Dual Role Device)

SDRAM

- Compatible with JEDEC standard LPDDR2/LPDDR3/DDR3/DDR3L SDRAM
- Up to 2GB address space
- 16 address signal lines and 3 bank signal lines
- 32-bit bus width
- Support Memory Dynamic Frequency Scale
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Random read or write operation is supported

NAND Flash

- Up to 4 flash chips
- 8-bit data BUS width
- 64-bit ECC per 1024 bytes
- Support 1024,2048,4096,8192,16K bytes size per page
- Support SDR,ONFI DDR and Toggle DDR NAND

SD/MMC Interface

- Up to three SD/MMC controllers
- 4/8-bit SD,SDIO,MMC mode
- Compatible with eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card

specification V2.0

- Data rate up to 100Mbps
- Support SDIO suspend and resume operation
- Support hardware CRC generation and error detection
- Support SDIO interrupt detection
- Support block size from 1 to 65535 bytes

2.4. System Peripheral

Timer

- Up to two timers
- 33-bit Audio/Video Sync counters
- One watchdog to generate reset signal or interrupts
- 24MHz or Internal OSC clock input

High Speed Timer

- Counters up to 56bits
- Clock source is synchronized with AHB clock, much more accurate than other timers

OSC24M

- Support 1.8v oscillator
- Support internal RC oscillator

GIC

- Support 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 168 SPIs(Shared Peripheral Interrupts)

DMA

- 8-channel DMA
- Flexible data width of 8/16/32 bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

CCU

- 11 PLLs
- Support a 24MHz oscillator and an on-chip RC oscillator
- Clock configuration for corresponding modules
- Support software-controlled clock gating and software-controlled reset for corresponding modules

PWM

- Up to two PWM channels
- Support outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

Security System

- Support symmetrical algorithm: AES, DES, TDES
- Support asymmetrical algorithm:RSA512/1024/2048/3072-bits
- Support hash algorithm:SHA-1/SHA-224/SHA-256, MD5
- 160-bits hardware PRNG with 192-bits seed
- 256-bits TRNG
- 32-bits hardware CRC
- Support ECB,CBC,CTR modes for DES/TDES

- Support ECB, CBC, CTR,CTS modes for AES 128/192/256-bits
- Support 2k-bits EFUSE for chip ID and security application

TrustZone

- Support TrustZone technology
- Support 96KB security SRAM

CPU Configuration

- Support power clamp
- Flexible CPU configuration

Power Management

- Support DVFS for CPU frequency and voltage adjustment
- Flexible clock gate and module reset
- Support dynamic frequency adjustment for external DRAM
- Support multiple power domains

2.5. Display Subsystem

Display Engine2.0

- Input layer size up to 2048x2048, and output size up to 2048x2048
- Support four alpha blending channel for main display, two channel for aux display
- Support four overlay layers in each channel, and has a independent scaler
- Support potter-duff compatible blending operation
- Support input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB8888/ARGB4444/ARGB1555 and RGB565
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Support display enhancement 2.0 for excellent display experience
 - Adaptive edge sharpening
 - Adaptive color enhancement
 - Adaptive contrast enhancement and fresh tone rectify
- Support write back & rotation for high efficient dual display and miracast

Video Output

- Support two independent display channels
- Support RGB(24bits) up to 1920x1200@60Hz resolution
- Support RGB666/656 ditcher function
- Support LVDS up to 1366x768@60Hz resolution
- Support 4-lane MIPI DSI(V1.0) up to 1920x1200@60Hz resolution
- Support HDMI V1.4 output with HDCP1.2

2.6. Video Engine

Video Decoding

- Support video playback up to 1080p@60ps
- Support multi-format video playback, including MPEG1/2, MPEG4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP,VP8, WMV9/VC1, JPEG/MJPEG, etc
- HEVC/H.265 decoder(software),Main Profile,1080p@30fps

Video Encoding

- Support H.264 video encoding up to 1080p@60fps,720p@120fps
- JPEG baseline: picture size up to 8192x8192

- Support input picture size up to 4800x4800
- Support input format: tiled(128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Support rotated input

2.7. Image Subsystem

CSI

- Support 10-bits parallel camera sensor
- Support up to 5M pixel camera sensor
- Support video shot up to 720p@30fps
- Support CCIR656 protocol for NTSC and PAL
- Support ITU-R BT.656 time-multiplexed format

MIPI CSI

- Compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00.00
- 4-lane MIPI CSI
- Up to 1Gbps per Lane in HS Transmission
- Maximum to 8M@30fps with 4 data lane
- Support video shot up to 1080p@60fps
- Supports format: YUV422-8bit/10bit,YUV420-8bit/10bit,RAW-8,RAW-10, RAW-12,RGB888,RGB565

ISP

- Support input formats:8/10-bits RAW RGB,8-bits YCbCr
- Support output formats: YCbCr420 semi-planar,YCrCb420 semi-planar, YCbCr422 semi-planar,YCrCb422 semi-planar,YUV420 planar,YUV422 Planar
- Support image mirror flip and rotation
- Support two output channels
- Speed up to 8MPixels@30fps
- Defect pixel correction
- Super lens shading correction
- Anisotropic non-linear Bayer interpolation with false color suppression
- Programmable color correction
- Advanced contrast enhance and sharpening
- Advanced saturation adjust
- Advanced spatial(2D) de-noise filter
- Advanced chrominance noise reduction
- Zone-based AE/AF/AWB statistics
- Anti-flick detection statistics
- Histogram statistics

2.8. External Peripherals

USB

- USB 2.0 DRD
 - Complies with USB2.0 Specification
 - Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) in host mode
 - Up to 10 User-Configurable Endpoints
 - Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Two EHCI/OHCI compliant Host SIE multiplexed with one USB 2.0 analog PHY, one HSIC PHY

- Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) Device
- An internal DMA Controller for data transfer with memory

EMAC

- Support 10/100/1000Mbps data transfer rate
- Support MII/RGMII PHY interface
- Support full-duplex and half-duplex operation
- Programmable frame length
- Flexible address filtering modes
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Programmable Inter Frame Gap (40-96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes

ADC

- LRADC with 6-bit resolution
- Support hold key and continuous key
- Support single key, normal key and continuous key

Digital Audio

- Support PCM/I2S
 - I2S and PCM are configurable through software
 - Support I2S formats: normal, left-justified, right-justified
 - Audio data resolution:16bits, 20bits, 24bits
 - Audio sample rate up to 192KHz
 - Master and slave work mode are configurable
- Support TDM(Time Division Multiplexing)
 - Master/Slave mode
 - Audio sample resolution from 8bits to 32bits
 - Sample rate from 8KHz to 192KHz
 - 4 data output pin
 - DMA-based or interrupt-based operation

CIR

- A flexible receiver for IR remote
- Programmable FIFO thresholds

UART

- Up to six UART controllers
- 64-Bytes Transmit and receive data FIFOs for all UART
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association(IrDA) 1.0 SIR
- Interrupt support for FIFOs,Status Change

SPI

- Up to two SPI controllers
- Master/Slave configurable
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation

TWI

- Up to four TWI(Two Wire Interface) controllers
- Support Standard mode(up to 100K bps) and Fast mode(up to 400K bps)

- Master/Slave configurable
- Allows 10-bit addressing transactions

RSB™(Reduced Serial Bus)

- A simplified two wire protocol
- Support master mode
- Support multi-slaves
- Speed up to 20Mbps

2.9. Package

- FBGA 345 balls,0.65mm ball pitch,14mm x14mm

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3. BLOCK DIAGRAM

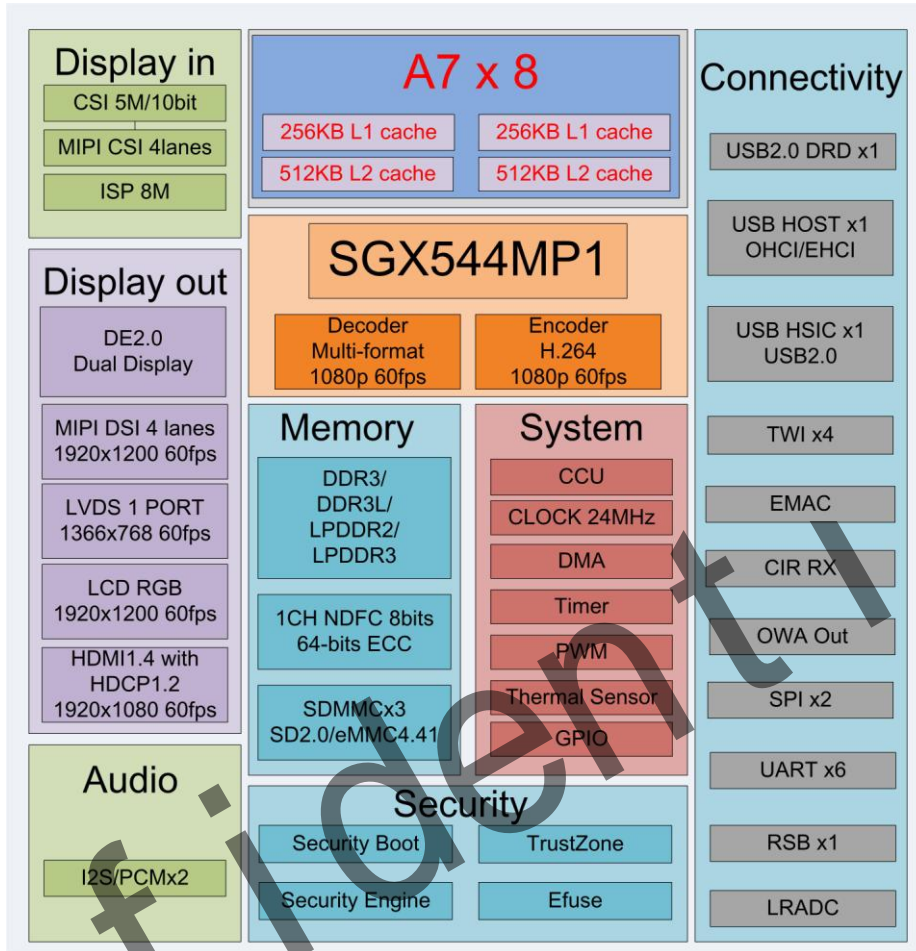


Figure 3-1. A83T Block Diagram

4. PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Table 4-1 lists the characteristics of A83T Pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.



NOTES

- 1) **Default Function** defines the default function of each pin, especially for pins with multiplexing functions;
- 2) **Type** defines the signal direction: I (Input), O (Output), I/O (Input / Output), A (Analog), P (Power), G (Ground);
- 3) **Reset State** defines the state of the terminal at reset: Z for high-impedance, F for Multiplexing Function Pin ;
- 4) **Default Pull Up/Down** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;
- 5) **Buffer Strength** defines drive strength of the associated output buffer. It is tested in the condition that VCC= 3.3V, strength=MAX;

Table 4-1 Pin Characteristics

| Ball# | Pin Name ^o | Default Function ^o | Type ^o | Reset State ^o | Default Pull Up/Down ^o | Buffer Strength ^o (mA) |
|-------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| DRAM | | | | | | |
| N4 | SA0 | DRAM | O | Z | - | - |
| M5 | SA1 | DRAM | O | Z | - | - |
| M4 | SA2 | DRAM | O | Z | - | - |
| L3 | SA3 | DRAM | O | Z | - | - |
| K3 | SA4 | DRAM | O | Z | - | - |
| J3 | SA5 | DRAM | O | Z | - | - |
| H2 | SA6 | DRAM | O | Z | - | - |
| H3 | SA7 | DRAM | O | Z | - | - |
| G3 | SA8 | DRAM | O | Z | - | - |
| G4 | SA9 | DRAM | O | Z | - | - |
| P3 | SA10 | DRAM | O | Z | - | - |
| U3 | SA11 | DRAM | O | Z | - | - |
| R5 | SA12 | DRAM | O | Z | - | - |
| G5 | SA13 | DRAM | O | Z | - | - |
| V4 | SA14 | DRAM | O | Z | - | - |
| R4 | SA15 | DRAM | O | Z | - | - |
| D6 | SADBG | DRAM | A | Z | - | - |
| G2 | SBA0 | DRAM | O | Z | - | - |
| T4 | SBA1 | DRAM | O | Z | - | - |
| G1 | SBA2 | DRAM | O | Z | - | - |
| F2 | SCAS | DRAM | O | Z | - | - |
| J1 | SCK | DRAM | O | Z | - | - |
| J2 | SCKB | DRAM | O | Z | - | - |
| J4 | SCKE0 | DRAM | O | Z | - | - |
| J5 | SCKE1 | DRAM | O | Z | - | - |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|-------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| K2 | SCS0 | DRAM | O | Z | - | - |
| K4 | SCS1 | DRAM | O | Z | - | - |
| E6 | SDDBG0 | DRAM | A | Z | - | - |
| D7 | SDDBG1 | DRAM | A | Z | - | - |
| R2 | SDQ0 | DRAM | I/O | Z | - | - |
| R1 | SDQ1 | DRAM | I/O | Z | - | - |
| P2 | SDQ2 | DRAM | I/O | Z | - | - |
| N3 | SDQ3 | DRAM | I/O | Z | - | - |
| M1 | SDQ4 | DRAM | I/O | Z | - | - |
| M2 | SDQ5 | DRAM | I/O | Z | - | - |
| M3 | SDQ6 | DRAM | I/O | Z | - | - |
| L2 | SDQ7 | DRAM | I/O | Z | - | - |
| Y1 | SDQ8 | DRAM | I/O | Z | - | - |
| W2 | SDQ9 | DRAM | I/O | Z | - | - |
| W1 | SDQ10 | DRAM | I/O | Z | - | - |
| V3 | SDQ11 | DRAM | I/O | Z | - | - |
| U2 | SDQ12 | DRAM | I/O | Z | - | - |
| T3 | SDQ13 | DRAM | I/O | Z | - | - |
| T2 | SDQ14 | DRAM | I/O | Z | - | - |
| T1 | SDQ15 | DRAM | I/O | Z | - | - |
| E2 | SDQ16 | DRAM | I/O | Z | - | - |
| D2 | SDQ17 | DRAM | I/O | Z | - | - |
| D1 | SDQ18 | DRAM | I/O | Z | - | - |
| D3 | SDQ19 | DRAM | I/O | Z | - | - |
| A2 | SDQ20 | DRAM | I/O | Z | - | - |
| B2 | SDQ21 | DRAM | I/O | Z | - | - |
| B1 | SDQ22 | DRAM | I/O | Z | - | - |
| A3 | SDQ23 | DRAM | I/O | Z | - | - |
| A4 | SDQ24 | DRAM | I/O | Z | - | - |
| B4 | SDQ25 | DRAM | I/O | Z | - | - |
| C4 | SDQ26 | DRAM | I/O | Z | - | - |
| B5 | SDQ27 | DRAM | I/O | Z | - | - |
| C6 | SDQ28 | DRAM | I/O | Z | - | - |
| A7 | SDQ29 | DRAM | I/O | Z | - | - |
| B8 | SDQ30 | DRAM | I/O | Z | - | - |
| B7 | SDQ31 | DRAM | I/O | Z | - | - |
| R3 | SDQM0 | DRAM | O | Z | - | - |
| Y2 | SDQM1 | DRAM | O | Z | - | - |
| F3 | SDQM2 | DRAM | O | Z | - | - |
| B3 | SDQM3 | DRAM | O | Z | - | - |
| N1 | SDQS0 | DRAM | I/O | Z | - | - |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|----------------------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| N2 | SDQS0B | DRAM | I/O | Z | - | - |
| V1 | SDQS1 | DRAM | I/O | Z | - | - |
| V2 | SDQS1B | DRAM | I/O | Z | - | - |
| C1 | SDQS2 | DRAM | I/O | Z | - | - |
| C2 | SDQS2B | DRAM | I/O | Z | - | - |
| B6 | SDQS3 | DRAM | I/O | Z | - | - |
| A6 | SDQS3B | DRAM | I/O | Z | - | - |
| E3 | SODT0 | DRAM | O | Z | - | - |
| F4 | SODT1 | DRAM | O | Z | - | - |
| D4 | SRAS | DRAM | O | Z | - | - |
| C5 | SRST | DRAM | O | Z | - | - |
| K1 | SVREF | DRAM | P | Z | - | - |
| F1 | SWE | DRAM | O | Z | - | - |
| T5 | SZQ | DRAM | A | Z | - | - |
| E7,F7,R6,J6,K6,L6,M6,N6,P6 | VCC-DRAM | POWER | P | - | - | - |
| N8 | VDD-SPLL | POWER | P | - | - | - |
| GPIO B | | | | | | |
| D10 | PB0 | GPIO | I/O | Z | NO PULL | 20 |
| E10 | PB1 | GPIO | I/O | Z | NO PULL | 20 |
| B11 | PB2 | GPIO | I/O | Z | NO PULL | 20 |
| B10 | PB3 | GPIO | I/O | Z | NO PULL | 20 |
| C9 | PB4 | GPIO | I/O | Z | NO PULL | 20 |
| A10 | PB5 | GPIO | I/O | Z | NO PULL | 20 |
| E9 | PB6 | GPIO | I/O | Z | NO PULL | 20 |
| B9 | PB7 | GPIO | I/O | Z | NO PULL | 20 |
| C8 | PB8 | GPIO | I/O | Z | NO PULL | 20 |
| A9 | PB9 | GPIO | I/O | Z | NO PULL | 20 |
| D9 | PB10 | GPIO | I/O | Z | NO PULL | 20 |
| F9,L13,T7 | VCC-IO | POWER | P | - | - | - |
| GPIO C | | | | | | |
| Y13 | PC0 | GPIO | I/O | Z | NO PULL | 20 |
| V12 | PC1 | GPIO | I/O | Z | NO PULL | 20 |
| AA13 | PC2 | GPIO | I/O | Z | NO PULL | 20 |
| W12 | PC3 | GPIO | I/O | Z | Pull-up | 20 |
| Y12 | PC4 | GPIO | I/O | Z | Pull-up | 20 |
| AA12 | PC5 | GPIO | I/O | Z | NO PULL | 20 |
| W11 | PC6 | GPIO | I/O | Z | Pull-up | 20 |
| Y11 | PC7 | GPIO | I/O | Z | Pull-up | 20 |
| T10 | PC8 | GPIO | I/O | Z | NO PULL | 20 |
| U10 | PC9 | GPIO | I/O | Z | NO PULL | 20 |
| V10 | PC10 | GPIO | I/O | Z | NO PULL | 20 |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|---------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| W10 | PC11 | GPIO | I/O | Z | NO PULL | 20 |
| Y10 | PC12 | GPIO | I/O | Z | NO PULL | 20 |
| AA10 | PC13 | GPIO | I/O | Z | NO PULL | 20 |
| T9 | PC14 | GPIO | I/O | Z | NO PULL | 20 |
| V9 | PC15 | GPIO | I/O | Z | NO PULL | 20 |
| W9 | PC16 | GPIO | I/O | Z | NO PULL | 20 |
| Y9 | PC17 | GPIO | I/O | Z | Pull-up | 20 |
| AA9 | PC18 | GPIO | I/O | Z | Pull-up | 20 |
| GPIO D | | | | | | |
| A20 | PD2 | GPIO | I/O | Z | NO PULL | 20 |
| B20 | PD3 | GPIO | I/O | Z | NO PULL | 20 |
| D18 | PD4 | GPIO | I/O | Z | NO PULL | 20 |
| D19 | PD5 | GPIO | I/O | Z | NO PULL | 20 |
| B21 | PD6 | GPIO | I/O | Z | NO PULL | 20 |
| C20 | PD7 | GPIO | I/O | Z | NO PULL | 20 |
| C21 | PD10 | GPIO | I/O | Z | NO PULL | 20 |
| D20 | PD11 | GPIO | I/O | Z | NO PULL | 20 |
| D21 | PD12 | GPIO | I/O | Z | NO PULL | 20 |
| E19 | PD13 | GPIO | I/O | Z | NO PULL | 20 |
| E20 | PD14 | GPIO | I/O | Z | NO PULL | 20 |
| F18 | PD15 | GPIO | I/O | Z | NO PULL | 20 |
| A15 | PD18 | GPIO | I/O | Z | NO PULL | 20 |
| B15 | PD19 | GPIO | I/O | Z | NO PULL | 20 |
| A16 | PD20 | GPIO | I/O | Z | NO PULL | 20 |
| B16 | PD21 | GPIO | I/O | Z | NO PULL | 20 |
| B17 | PD22 | GPIO | I/O | Z | NO PULL | 20 |
| C16 | PD23 | GPIO | I/O | Z | NO PULL | 20 |
| A18 | PD24 | GPIO | I/O | Z | NO PULL | 20 |
| B18 | PD25 | GPIO | I/O | Z | NO PULL | 20 |
| A19 | PD26 | GPIO | I/O | Z | NO PULL | 20 |
| B19 | PD27 | GPIO | I/O | Z | NO PULL | 20 |
| C17 | PD28 | GPIO | I/O | Z | NO PULL | 20 |
| C18 | PD29 | GPIO | I/O | Z | NO PULL | 20 |
| F13,F14 | VCC-PD | POWER | P | - | - | - |
| F12 | VCC18-LVDS | POWER | P | - | - | - |
| GPIO E | | | | | | |
| E15 | PE0 | GPIO | I/O | Z | NO PULL | 20 |
| E16 | PE1 | GPIO | I/O | Z | NO PULL | 20 |
| D16 | PE2 | GPIO | I/O | Z | NO PULL | 20 |
| C15 | PE3 | GPIO | I/O | Z | NO PULL | 20 |
| D15 | PE4 | GPIO | I/O | Z | NO PULL | 20 |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|---------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| F15 | PE5 | GPIO | I/O | Z | NO PULL | 20 |
| E13 | PE6 | GPIO | I/O | Z | NO PULL | 20 |
| D13 | PE7 | GPIO | I/O | Z | NO PULL | 20 |
| B14 | PE8 | GPIO | I/O | Z | NO PULL | 20 |
| F17 | PE9 | GPIO | I/O | Z | NO PULL | 20 |
| C14 | PE10 | GPIO | I/O | Z | NO PULL | 20 |
| E12 | PE11 | GPIO | I/O | Z | NO PULL | 20 |
| C13 | PE12 | GPIO | I/O | Z | NO PULL | 20 |
| D12 | PE13 | GPIO | I/O | Z | NO PULL | 20 |
| C12 | PE14 | GPIO | I/O | Z | NO PULL | 20 |
| B13 | PE15 | GPIO | I/O | Z | NO PULL | 20 |
| A13 | PE16 | GPIO | I/O | Z | NO PULL | 20 |
| B12 | PE17 | GPIO | I/O | Z | NO PULL | 20 |
| A12 | PE18 | GPIO | I/O | Z | NO PULL | 20 |
| C10 | PE19 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO F | | | | | | |
| Y5 | PF0 | GPIO | I/O | F | NO PULL | 20 |
| Y4 | PF1 | GPIO | I/O | F | NO PULL | 20 |
| AA4 | PF2 | GPIO | I/O | Z | NO PULL | 20 |
| W4 | PF3 | GPIO | I/O | F | NO PULL | 20 |
| AA3 | PF4 | GPIO | I/O | Z | NO PULL | 20 |
| Y3 | PF5 | GPIO | I/O | F | NO PULL | 20 |
| AA2 | PF6 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO G | | | | | | |
| K17 | PG0 | GPIO | I/O | Z | NO PULL | 20 |
| K18 | PG1 | GPIO | I/O | Z | NO PULL | 20 |
| L19 | PG2 | GPIO | I/O | Z | NO PULL | 20 |
| M16 | PG3 | GPIO | I/O | Z | NO PULL | 20 |
| M17 | PG4 | GPIO | I/O | Z | NO PULL | 20 |
| M18 | PG5 | GPIO | I/O | Z | NO PULL | 20 |
| M19 | PG6 | GPIO | I/O | Z | NO PULL | 20 |
| N16 | PG7 | GPIO | I/O | Z | NO PULL | 20 |
| N18 | PG8 | GPIO | I/O | Z | NO PULL | 20 |
| N19 | PG9 | GPIO | I/O | Z | NO PULL | 20 |
| N20 | PG10 | GPIO | I/O | Z | NO PULL | 20 |
| N21 | PG11 | GPIO | I/O | Z | NO PULL | 20 |
| P19 | PG12 | GPIO | I/O | Z | NO PULL | 20 |
| R18 | PG13 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO H | | | | | | |
| U9 | PH0 | GPIO | I/O | Z | NO PULL | 20 |
| W8 | PH1 | GPIO | I/O | Z | NO PULL | 20 |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|-----------------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| Y8 | PH2 | GPIO | I/O | Z | NO PULL | 20 |
| AA7 | PH3 | GPIO | I/O | Z | NO PULL | 20 |
| Y7 | PH4 | GPIO | I/O | Z | NO PULL | 20 |
| W7 | PH5 | GPIO | I/O | Z | NO PULL | 20 |
| V7 | PH6 | GPIO | I/O | Z | NO PULL | 20 |
| AA6 | PH7 | GPIO | I/O | Z | NO PULL | 20 |
| U7 | PH8 | GPIO | I/O | Z | NO PULL | 20 |
| Y6 | PH9 | GPIO | I/O | Z | NO PULL | 20 |
| W6 | PH10 | GPIO | I/O | Z | NO PULL | 20 |
| V6 | PH11 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO L | | | | | | |
| AA15 | PL0 | GPIO | I/O | Z | Pull-up | 20 |
| W14 | PL1 | GPIO | I/O | Z | Pull-up | 20 |
| W16 | PL2 | GPIO | I/O | Z | NO PULL | 20 |
| V16 | PL3 | GPIO | I/O | Z | NO PULL | 20 |
| V15 | PL4 | GPIO | I/O | Z | NO PULL | 20 |
| W17 | PL5 | GPIO | I/O | Z | NO PULL | 20 |
| Y17 | PL6 | GPIO | I/O | Z | NO PULL | 20 |
| U16 | PL7 | GPIO | I/O | Z | NO PULL | 20 |
| AA18 | PL8 | GPIO | I/O | Z | NO PULL | 20 |
| Y18 | PL9 | GPIO | I/O | Z | NO PULL | 20 |
| W18 | PL10 | GPIO | I/O | Z | NO PULL | 20 |
| V18 | PL11 | GPIO | I/O | Z | NO PULL | 20 |
| AA19 | PL12 | GPIO | I/O | Z | NO PULL | 20 |
| T15 | VCC-PL | POWER | P | - | - | - |
| System Control | | | | | | |
| U15 | UBOOT | - | I | - | Pull-up | - |
| W5 | JTAGSEL | - | I | - | Pull-up | - |
| Y14 | TEST | - | I | - | Pull-down | - |
| Y16 | NMI | - | I | Z | NO PULL | - |
| AA16 | RESET | - | I | Z | NO PULL | - |
| U13 | VCC18-EFUSE | - | P | - | - | - |
| HDMI | | | | | | |
| J18 | HHPD | - | A | - | - | - |
| L20 | HTX0N | - | A | - | - | - |
| K19 | HTX0P | - | A | - | - | - |
| K21 | HTX1N | - | A | - | - | - |
| K20 | HTX1P | - | A | - | - | - |
| J21 | HTX2N | - | A | - | - | - |
| J20 | HTX2P | - | A | - | - | - |
| M21 | HTXCN | - | A | - | - | - |

| Ball# | Pin Name [®] | Default Function [®] | Type [®] | Reset State [®] | Default Pull Up/Down [®] | Buffer Strength [®] (mA) |
|-------------|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| M20 | HTXCP | - | A | - | - | - |
| K14 | VCC18-HDMI | - | P | - | - | - |
| K13 | VDD09-HDMI | - | P | - | - | - |
| USB | | | | | | |
| W20 | USB0_DM | - | A | - | - | - |
| W21 | USB0_DP | - | A | - | - | - |
| Y21 | USB0_ID | - | A | - | - | - |
| Y19 | USB0_VBUS | - | A | - | - | - |
| AA20 | USB1_DM | - | A | - | - | - |
| Y20 | USB1_DP | - | A | - | - | - |
| R16 | VCC33-USB | - | P | - | - | - |
| P13 | VDD09-USB | - | P | - | - | - |
| HSIC | | | | | | |
| V21 | HSIC-DATA | - | A | - | - | - |
| V20 | HSIC-STRB | - | A | - | - | - |
| P14 | VCC12-HSIC | - | P | - | - | - |
| ADC | | | | | | |
| W15 | LRADC0 | - | A | - | - | - |
| T14 | GND-ADC | - | G | - | - | - |
| MCSI | | | | | | |
| T21 | MCSI-CKN | - | A | - | - | - |
| T20 | MCSI-CKP | - | A | - | - | - |
| U19 | MCSI-DN0 | - | A | - | - | - |
| T19 | MCSI-DN1 | - | A | - | - | - |
| R21 | MCSI-DN2 | - | A | - | - | - |
| P20 | MCSI-DN3 | - | A | - | - | - |
| V19 | MCSI-DP0 | - | A | - | - | - |
| U20 | MCSI-DP1 | - | A | - | - | - |
| R20 | MCSI-DP2 | - | A | - | - | - |
| R19 | MCSI-DP3 | - | A | - | - | - |
| N13 | VCC18-MCSI | - | P | - | - | - |
| MDSI | | | | | | |
| G18 | MDSI-CKN | - | A | - | - | - |
| G19 | MDSI-CKP | - | A | - | - | - |
| H20 | MDSI-DN0 | - | A | - | - | - |
| G20 | MDSI-DN1 | - | A | - | - | - |
| F21 | MDSI-DN2 | - | A | - | - | - |
| F19 | MDSI-DN3 | - | A | - | - | - |
| J19 | MDSI-DP0 | - | A | - | - | - |
| H19 | MDSI-DP1 | - | A | - | - | - |
| G21 | MDSI-DP2 | - | A | - | - | - |

| Ball# | Pin Name [°] | Default Function [°] | Type [°] | Reset State [°] | Default Pull Up/Down [°] | Buffer Strength [°] (mA) |
|---|-----------------------|-------------------------------|-------------------|--------------------------|-----------------------------------|-----------------------------------|
| F20 | MDSI-DP3 | - | A | - | - | - |
| H13 | VCC18-MDSI | - | P | - | - | - |
| RTC&PLL | | | | | | |
| W13 | REXT | - | A | - | - | - |
| Y15 | RTC-VIO | - | P | - | - | - |
| U12 | X24MI | - | A | - | - | - |
| V13 | X24MO | - | A | - | - | - |
| Other | | | | | | |
| M10 | VDDFB-CPUA | - | I/O | - | - | - |
| J12 | VDDFB-CPUB | - | I/O | - | - | - |
| Power | | | | | | |
| T12 | VCC18-PLL | - | P | - | - | - |
| T13 | VCC18-ADC | - | P | - | - | - |
| F8,L14,T8 | VDD18 | - | P | - | - | - |
| L9,L10,L11,L12,M9,M11,M12,M13,M14 | VDD-CPUA | - | P | - | - | - |
| F10,F11,H9,H10,H11,J9,J10,J11 | VDD-CPUB | - | P | - | - | - |
| R17,T17 | VDD-CPUS | - | P | - | - | - |
| P9,P10,P11,T11 | VDD-GPU | - | P | - | - | - |
| J14,J16,K16 | VDD-SYS | - | P | - | - | - |
| A1,A21,C7,C11,F5,G6,G16,G17,H8,H12,H14,H16,J8,J13,J17,K5,K8,K9,K10,K11,K12,L8,L16,M8,N5,N9,N10,N11,N12,N14,N17,P8,P12,P16,H6,U6,T18,A1,AA21 | GND(39) | - | G | - | - | - |

4.2. GPIO MULTIPLEXING FUNCTIONS

The following table provides a description of the A83T GPIO multiplexing functions.

Table 4-2 Multiplexing Functions

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|------------|------------|------------|
| PB0 | GPIO | I/O | DIS | Z | UART2_TX | JTAG_MS0 | - | - | PB_EINT0 |
| PB1 | | I/O | DIS | Z | UART2_RX | JTAG_CK0 | - | - | PB_EINT1 |
| PB2 | | I/O | DIS | Z | UART2_RTS | JTAG_DO0 | - | - | PB_EINT2 |
| PB3 | | I/O | DIS | Z | UART2_CTS | JTAG_DIO | - | - | PB_EINT3 |
| PB4 | | I/O | DIS | Z | I2S0_LRCK | TDM_LRCK | - | - | PB_EINT4 |

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|-----------------------|------------|------------|
| PB5 | | I/O | DIS | Z | I2S0_BCLK | TDM_BCLK | - | - | PB_EINT5 |
| PB6 | | I/O | DIS | Z | I2S0_DOUT | TDM_DOUT | - | - | PB_EINT6 |
| PB7 | | I/O | DIS | Z | I2S0_DIN | TDM_DIN | - | - | PB_EINT7 |
| PB8 | | I/O | DIS | Z | I2S0_MCLK | TDM_MCLK | - | - | PB_EINT8 |
| PB9 | | I/O | DIS | Z | UART0_TX | - | - | - | PB_EINT9 |
| PB10 | | I/O | DIS | Z | UART0_RX | - | - | - | PB_EINT10 |
| PC0 | | I/O | DIS | Z | NAND_WE | SPI0_MOSI | - | - | - |
| PC1 | | I/O | DIS | Z | NAND_ALE | SPI0_MISO | - | - | - |
| PC2 | | I/O | DIS | Z | NAND_CLE | SPI0_CLK | - | - | - |
| PC3 | | I/O | DIS | Pull-up | NAND_CE1 | SPI0_CS | - | - | - |
| PC4 | | I/O | DIS | Pull-up | NAND_CE0 | - | - | - | - |
| PC5 | | I/O | DIS | Z | NAND_RE | SDC2_CLK | - | - | - |
| PC6 | | I/O | DIS | Pull-up | NAND_RB0 | SDC2_CMD | - | - | - |
| PC7 | | I/O | DIS | Pull-up | NAND_RB1 | - | - | - | - |
| PC8 | | I/O | DIS | Z | NAND_DQ0 | SDC2_D0 | - | - | - |
| PC9 | GPIO | I/O | DIS | Z | NAND_DQ1 | SDC2_D1 | - | - | - |
| PC10 | | I/O | DIS | Z | NAND_DQ2 | SDC2_D2 | - | - | - |
| PC11 | | I/O | DIS | Z | NAND_DQ3 | SDC2_D3 | - | - | - |
| PC12 | | I/O | DIS | Z | NAND_DQ4 | SDC2_D4 | - | - | - |
| PC13 | | I/O | DIS | Z | NAND_DQ5 | SDC2_D5 | - | - | - |
| PC14 | | I/O | DIS | Z | NAND_DQ6 | SDC2_D6 | - | - | - |
| PC15 | | I/O | DIS | Z | NAND_DQ7 | SDC2_D7 | - | - | - |
| PC16 | | I/O | DIS | Z | NAND_DQS | SDC2_RST | - | - | - |
| PC17 | | I/O | DIS | Pull-up | NAND_CE2 | - | - | - | - |
| PC18 | | I/O | DIS | Pull-up | NAND_CE3 | - | - | - | - |
| PD2 | | I/O | DIS | Z | LCD_D2 | - | RGMII-RXD3 /MII-RXD3 | - | - |
| PD3 | | I/O | DIS | Z | LCD_D3 | - | RGMII-RXD2 /MII-RXD2 | - | - |
| PD4 | | I/O | DIS | Z | LCD_D4 | - | RGMII-RXD1 /MII-RXD1 | - | - |
| PD5 | | I/O | DIS | Z | LCD_D5 | - | RGMII-RXD0 /MII-RXD0 | - | - |
| PD6 | | I/O | DIS | Z | LCD_D6 | - | RGMII-RXCK /MII-RXCK | - | - |
| PD7 | | I/O | DIS | Z | LCD_D7 | - | RGMII-RXCTL/MII-RXDV | - | - |
| PD10 | GPIO | I/O | DIS | Z | LCD_D10 | - | RGMII-NULL /MII-RXERR | - | - |
| PD11 | | I/O | DIS | Z | LCD_D11 | - | RGMII-TXD3 /MII-TXD3 | - | - |
| PD12 | | I/O | DIS | Z | LCD_D12 | - | RGMII-TXD2 /MII-TXD2 | - | - |
| PD13 | | I/O | DIS | Z | LCD_D13 | - | RGMII-TXD1 /MII-TXD1 | - | - |
| PD14 | | I/O | DIS | Z | LCD_D14 | - | RGMII-TXD0 /MII-TXD0 | - | - |
| PD15 | | I/O | DIS | Z | LCD_D15 | - | RGMII-NULL /MII-CRS | - | - |

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|------------------------|------------|------------|
| PD18 | | I/O | DIS | Z | LCD_D18 | LVDS_VP0 | RGMII-TXCK /MII-TXCK | - | - |
| PD19 | | I/O | DIS | Z | LCD_D19 | LVDS_VN0 | RGMII-TXCTL/MII-TXEN | - | - |
| PD20 | | I/O | DIS | Z | LCD_D20 | LVDS_VP1 | RGMII-NULLEN/MII-TXERR | - | - |
| PD21 | | I/O | DIS | Z | LCD_D21 | LVDS_VN1 | RGMII-CLKIN/MII-COL | - | - |
| PD22 | | I/O | DIS | Z | LCD_D22 | LVDS_VP2 | EMDC | - | - |
| PD23 | | I/O | DIS | Z | LCD_D23 | LVDS_VN2 | EMDIO | - | - |
| PD24 | | I/O | DIS | Z | LCD_CLK | LVDS_VPC | - | - | - |
| PD25 | | I/O | DIS | Z | LCD_DE | LVDS_VNC | - | - | - |
| PD26 | | I/O | DIS | Z | LCD_HSYNC | LVDS_VP3 | - | - | - |
| PD27 | | I/O | DIS | Z | LCD_VSYNC | LVDS_VP3 | - | - | - |
| PD28 | | I/O | DIS | Z | PWM | - | - | - | - |
| PD29 | | I/O | DIS | Z | - | - | - | - | - |
| PE0 | | GPIO | I/O | DIS | Z | CSI_PCLK | - | CCIR-CLK | - |
| PE1 | I/O | | DIS | Z | CSI_MCLK | - | CCIR-DE | - | - |
| PE2 | I/O | | DIS | Z | CSI_HSYNC | - | CCIR-HSYNC | - | - |
| PE3 | I/O | | DIS | Z | CSI_VSYNC | - | CCIR-VSYNC | - | - |
| PE4 | I/O | | DIS | Z | CSI_D0 | - | - | - | - |
| PE5 | I/O | | DIS | Z | CSI_D1 | - | - | - | - |
| PE6 | I/O | | DIS | Z | CSI_D2 | - | CCIR-D0 | - | - |
| PE7 | I/O | | DIS | Z | CSI_D3 | - | CCIR-D1 | - | - |
| PE8 | I/O | | DIS | Z | CSI_D4 | - | CCIR-D2 | - | - |
| PE9 | I/O | | DIS | Z | CSI_D5 | - | CCIR-D3 | - | - |
| PE10 | I/O | | DIS | Z | CSI_D6 | UART4_TX | CCIR-D4 | - | - |
| PE11 | I/O | | DIS | Z | CSI_D7 | UART4_RX | CCIR-D5 | - | - |
| PE12 | I/O | | DIS | Z | CSI_D8 | UART4_RTS | CCIR-D6 | - | - |
| PE13 | I/O | | DIS | Z | CSI_D9 | UART4_CTS | CCIR-D7 | - | - |
| PE14 | I/O | | DIS | Z | CSI_SCK | TWI2_SCK | - | - | - |
| PE15 | I/O | | DIS | Z | CSI_SDA | TWI2_SDA | - | - | - |
| PE16 | I/O | | DIS | Z | - | - | - | - | - |
| PE17 | I/O | | DIS | Z | - | - | - | - | - |
| PE18 | I/O | | DIS | Z | - | OWA_OUT | - | - | - |
| PE19 | I/O | DIS | Z | - | - | - | - | - | |
| PF0 | GPIO | I/O | DIS | F | SDC0_D1 | JTAG_MS1 | - | - | - |
| PF1 | | I/O | DIS | F | SDC0_D0 | JTAG_DI1 | - | - | - |
| PF2 | | I/O | DIS | Z | SDC0_CLK | UART0_TX | - | - | - |
| PF3 | | I/O | DIS | F | SDC0_CMD | JTAG_DO1 | - | - | - |
| PF4 | | I/O | DIS | Z | SDC0_D3 | UART0_RX | - | - | - |
| PF5 | | I/O | DIS | F | SDC0_D2 | JTAG_CK1 | - | - | - |
| PF6 | | I/O | DIS | Z | - | - | - | - | - |
| PG0 | GPIO | I/O | DIS | Z | SDC1_CLK | - | - | - | PG_EINT0 |

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|------------|-------------|-------------|
| PG1 | | I/O | DIS | Z | SDC1_CMD | - | - | - | PG_EINT1 |
| PG2 | | I/O | DIS | Z | SDC1_D0 | - | - | - | PG_EINT2 |
| PG3 | | I/O | DIS | Z | SDC1_D1 | - | - | - | PG_EINT3 |
| PG4 | | I/O | DIS | Z | SDC1_D2 | - | - | - | PG_EINT4 |
| PG5 | | I/O | DIS | Z | SDC1_D3 | - | - | - | PG_EINT5 |
| PG6 | | I/O | DIS | Z | UART1_TX | SPI1_CS | - | - | PG_EINT6 |
| PG7 | | I/O | DIS | Z | UART1_RX | SPI1_CLK | - | - | PG_EINT7 |
| PG8 | | I/O | DIS | Z | UART1_RTS | SPI1_MOSI | - | - | PG_EINT8 |
| PG9 | | I/O | DIS | Z | UART1_CTS | SPI1_MISO | - | - | PG_EINT9 |
| PG10 | | I/O | DIS | Z | I2S1_BCLK | UART3_TX | - | - | PG_EINT10 |
| PG11 | | I/O | DIS | Z | I2S1_LRCK | UART3_RX | - | - | PG_EINT11 |
| PG12 | | I/O | DIS | Z | I2S1_DOUT | UART3_RTS | - | - | PG_EINT12 |
| PG13 | | I/O | DIS | Z | I2S1_DIN | UART3_CTS | - | - | PG_EINT13 |
| PH0 | GPIO | I/O | DIS | Z | TWI0_SCK | - | - | - | PH_EINT0 |
| PH1 | | I/O | DIS | Z | TWI0_SDA | - | - | - | PH_EINT1 |
| PH2 | | I/O | DIS | Z | TWI1_SCK | - | - | - | PH_EINT2 |
| PH3 | | I/O | DIS | Z | TWI1_SDA | - | - | - | PH_EINT3 |
| PH4 | | I/O | DIS | Z | TWI2_SCK | - | - | - | PH_EINT4 |
| PH5 | | I/O | DIS | Z | TWI2_SDA | - | - | - | PH_EINT5 |
| PH6 | | I/O | DIS | Z | HSCL | - | - | - | PH_EINT6 |
| PH7 | | I/O | DIS | Z | HSDA | - | - | - | PH_EINT7 |
| PH8 | | I/O | DIS | Z | HCEC | - | - | - | PH_EINT8 |
| PH9 | | I/O | DIS | Z | - | - | - | - | PH_EINT9 |
| PH10 | | I/O | DIS | Z | - | - | - | - | PH_EINT10 |
| PH11 | I/O | DIS | Z | - | - | - | - | PH_EINT11 | |
| PL0 | GPIO | I/O | DIS | Pull-up | S_RSB_SCK | S_TWI_SCK | - | - | S_PL_EINT0 |
| PL1 | | I/O | DIS | Pull-up | S_RSB_SDA | S_TWI_SDA | - | - | S_PL_EINT1 |
| PL2 | | I/O | DIS | Z | S_UART_TX | - | - | - | S_PL_EINT2 |
| PL3 | | I/O | DIS | Z | S_UART_RX | - | - | - | S_PL_EINT3 |
| PL4 | | I/O | DIS | Z | S_JTAG_MS | - | - | - | S_PL_EINT4 |
| PL5 | | I/O | DIS | Z | S_JTAG_CK | - | - | - | S_PL_EINT5 |
| PL6 | | I/O | DIS | Z | S_JTAG_DO | - | - | - | S_PL_EINT6 |
| PL7 | | I/O | DIS | Z | S_JTAG_DI | - | - | - | S_PL_EINT7 |
| PL8 | | I/O | DIS | Z | S_TWI_SCK | - | - | - | S_PL_EINT8 |
| PL9 | | I/O | DIS | Z | S_TWI_SDA | - | - | - | S_PL_EINT9 |
| PL10 | | I/O | DIS | Z | S_PWM | - | - | - | S_PL_EINT10 |
| PL11 | | I/O | DIS | Z | - | - | - | - | S_PL_EINT11 |
| PL12 | I/O | DIS | Z | S_CIR_RX | - | - | - | S_PL_EINT12 | |

4.3. DETAILED PIN/SIGNAL DESCRIPTION

Table 4-3 shows the pin/signal description of A83T.

Table 4-3 Detailed Pin Description

| Pin/Signal Name | Description | Type |
|-----------------------|----------------------------|------|
| DRAM | | |
| SDQ[31:0] | DRAM DQ[31:0] | I/O |
| SDQS[3:0] | DRAM Data Strobe DQS[3:0] | I/O |
| SDQSB[3:0] | DRAM DQSB[3:0] | I/O |
| SDQM[3:0] | DRAM DQ Mask [3:0] | O |
| SCK | DRAM Clock | O |
| SCKB | DRAM CKB | O |
| SCKE[1:0] | DRAM Clock Enable [1:0] | O |
| SA[15:0] | DRAM data Address [15:0] | O |
| SWE | DRAM Write Enable | O |
| SCAS | DRAM Column Address Strobe | O |
| SRAS | DRAM Row Address Strobe | O |
| SCS[1:0] | DRAM Chip Select [1:0] | O |
| SBA[2:0] | DRAM Bank Address [2:0] | O |
| SODT[1:0] | DRAM ODT Control [1:0] | O |
| SRST | DRAM Reset | O |
| SZQ | DRAM ZQ Calibration | A |
| SVREF | DRAM Reference Input | P |
| VCC-DRAM | DRAM Power Supply | P |
| GND-DRAM | DRAM Ground | G |
| VDD-SPLL[2:0] | DLL Power Supply[2:0] | P |
| SDBG | DRAM DBG | A |
| System Control | | |
| UBOOT | UBOOT | I |
| JTAGSEL | JTAG Mode Select | I |
| TEST | TEST Signal | I |
| VCC18-EFUSE | eFUSE Power Supply | P |
| NMI | Non-Maskable Interrupt | I |
| RESET | RESET Signal | I |
| HDMI | | |
| HTX0P | TMDS Data 0 Positive | A |
| HTX0N | TMDS Data 0 Negative | A |
| HTX1P | TMDS Data 1 Positive | A |
| HTX1N | TMDS Data 1 Negative | A |
| HTX2P | TMDS Data 2 Positive | A |
| HTX2N | TMDS Data 2 Negative | A |

| Pin/Signal Name | Description | Type |
|-----------------|--------------------------------|------|
| HTXCP | TMDS Clock Positive | A |
| HTXCN | TMDS Clock Negative | A |
| VCC18-HDMI | HDMI Power Supply | P |
| VDD09-HDMI | HDMI Power Supply | P |
| HHPD | HDMI Hot Plug Detection signal | A |
| USB | | |
| USB0-DM | USB DM Signal | A |
| USB0-DP | USB DP Signal | A |
| USB0-ID | USB ID Signal | A |
| USB0-VBUS | USB VBUS Signal | A |
| USB1-DM | USB DM Signal | A |
| USB1-DP | USB DP Signal | A |
| VCC33-USB | USB Power Supply | P |
| VDD09-USB | USB Power Supply | P |
| HSIC | | |
| VCC12-HSIC | HSIC Power Supply | P |
| HSIC-STRB | USB HSIC Strobe Signal | A |
| HSIC-DATA | USB HSIC Data Signal | A |
| ADC | | |
| LRADC0 | LRADC input | A |
| VCC18-ADC | ADC Power Supply | P |
| MDSI | | |
| MDSI_DN0 | MIPI DSI Data 0 Negative | A |
| MDSI_DP0 | MIPI DSI Data 0 Positive | A |
| MDSI_DN1 | MIPI DSI Data 1 Negative | A |
| MDSI_DP1 | MIPI DSI Data 1 Positive | A |
| MDSI_DN2 | MIPI DSI Data 2 Negative | A |
| MDSI_DP2 | MIPI DSI Data 2 Positive | A |
| MDSI_DN3 | MIPI DSI Data 3 Negative | A |
| MDSI_DP3 | MIPI DSI Data 3 Positive | A |
| MDSI-CKN | MIPI DSI Clock Negative | A |
| MDSI-CKP | MIPI DSI Clock Positive | A |
| VCC18-MDSI | MIPI DSI Power Supply | P |
| MCSI | | |
| MCSI_DN0 | MIPI CSI Data 0 Negative | A |
| MCSI_DP0 | MIPI CSI Data 0 Positive | A |
| MCSI_DN1 | MIPI CSI Data 1 Negative | A |
| MCSI_DP1 | MIPI CSI Data 1 Positive | A |
| MCSI_DN2 | MIPI CSI Data 2 Negative | A |
| MCSI_DP2 | MIPI CSI Data 2 Positive | A |
| MCSI_DN3 | MIPI CSI Data 3 Negative | A |
| MCSI_DP3 | MIPI CSI Data 3 Positive | A |

| Pin/Signal Name | Description | Type |
|-------------------------|---------------------------------|------|
| MCSI-CKN | MIPI CSI Clock Negative | A |
| MCSI-CKP | MIPI CSI Clock Positive | A |
| VCC18-MCSI | MIPI CSI Power Supply | P |
| RTC&PLL | | |
| REXT | External Reference Register | A |
| RTC-VIO | Internal LDO Output Bypass | P |
| X24MI | Clock Input Of 24MHz Crystal | A |
| X24MO | Clock Output Of 24MHz Crystal | A |
| TEST | PLL Test Signal | I |
| VCC18-PLL | PLL Power Supply | P |
| SD /MMC(x=[2:0]) | | |
| SDCx_CMD | SDx/MMCx/SDIOx Command Signal | I/O |
| SDCx_CLK | SDx/MMCx/SDIOx Clock | O |
| SDC0_D[3:0] | SD0/MMC0/SDIO0 Data [3:0] | I/O |
| SDC1_D[3:0] | SD1/MMC1/SDIO1 Data [3:0] | I/O |
| SDC2_D[7:0] | SD2/MMC2/SDIO2 Data [7:0] | I/O |
| SDC2_RST | SD2/MMC2/SDIO2 Reset Signal | I/O |
| NAND FLASH | | |
| NAND_DQ[7:0] | NAND Flash Data Bit [7:0] | I/O |
| NAND_DQS | NAND Flash Data Strobe | I/O |
| NAND_WE | NAND Flash Write Enable | O |
| NAND_RE | NAND Flash chip Read Enable | O |
| NAND_ALE | NAND Flash Address Latch Enable | O |
| NAND_CLE | NAND Command Latch Enable | O |
| NAND_CE[3:0] | NAND Flash Chip Select [3:0] | O |
| NAND_RB[1:0] | NAND Flash Ready/Busy Bit | I |
| RSB | | |
| S_RSB_SCK | RSB Clock | I/O |
| S_RSB_SDA | RSB Data | I/O |
| Interrupt | | |
| PB_EINT[10:0] | GPIO B Interrupt | I/O |
| PG_EINT[13:0] | GPIO G Interrupt | I/O |
| PH_EINT[11:0] | GPIO H Interrupt | I/O |
| S_PL_EINT[12:0] | GPIO L Interrupt | I/O |
| PWM | | |
| S_PWM | PWM | O |
| PWM | PWM | O |
| IR | | |
| S_IR_RX | IR Data Receive | I |
| LCD | | |
| LCD0_D[23:0] | LCD Data Bit [23:0] | O |
| LCD_CLK | LCD Clock signal | O |

| Pin/Signal Name | Description | Type |
|-----------------------|---|------|
| LCD_DE | LCD Data Enable | O |
| LCD_HSYNC | LCD Horizontal SYNC | O |
| LCD_VSYNC | LCD Vertical SYNC | O |
| LVDS | | |
| LVDS_VP[3:0] | LVDS Data Positive Signal Output[3:0] | A |
| LVDS_VN[3:0] | LVDS Data Negative Signal Output[3:0] | A |
| LVDS_VPC | LVDS Clock Positive Signal Output | A |
| LVDS_VNC | LVDS Clock Negative Signal Output | A |
| I2S (x=[1:0]) | | |
| I2S0_MCLK | I2S 0 Master Clock (system clock) | O |
| I2Sx_BCLK | I2S Bit Clock | I/O |
| I2Sx_LRCK | I2S Left/Right Channel Select Clock | I/O |
| I2Sx_DIN | I2Sx Data Input | I |
| I2Sx_DOUT | I2Sx Data Output | O |
| CSI | | |
| CSI_PCLK | CSI Pixel Clock | I |
| CSI_MCLK | CSI Master Clock | O |
| CSI_HSYNC | CSI Horizontal SYNC | I |
| CSI_VSYNC | CSI Vertical SYNC | I |
| CSI_D[9:0] | CSI Data bit [9:0] | I |
| CSI_SCK | CSI Command Serial Clock Signal | O |
| CSI_SDA | CSI Command Serial Data Signal | I/O |
| EMAC | | |
| RGMII-RXD[3:0] | MII Receive Data Nibble Data Bit[3:0] | I |
| RGMII-RXCK | MII Receive Clock | I |
| RGMII-RXCTL/MII-RXDV | MII Receive Control/EMAC Receive Data Valid | I |
| MII-RXERR | MII Receive Error | I |
| RGMII-TXD[3:0] | MII Transmit Data Nibble Data Bit[3:0] | O |
| MII-CRS | MII Carrier Sense | I |
| RGMII-TXCK/MII-TXCK | MII Transmit Clock | O |
| RGMII-TXCTL/MII-TXEN | MII Transmit Control/MII Transmit Enable | O |
| MII-TXERR | MII Transmit Error | O |
| RGMII-CLKIN/MII-COL | MII Clock Input/EMAC Collision Detect | I |
| EMDC | MII Management Data Clock | O |
| EMDIO | MII Management Data Input/Output | I/O |
| SPI (x=[1:0]) | | |
| SPIx_CS | SPIx Chip Select signal | I/O |
| SPIx_CLK | SPI Clock signal | I/O |
| SPIx_MOSI | SPI Master data Out, Slave data In | I/O |
| SPIx_MISO | SPI Master data In, Slave data Out | I/O |
| UART (x=[4:0]) | | |
| UARTx_CTS | UART Data Clear To Send | I |

| Pin/Signal Name | Description | Type |
|----------------------|---------------------------|------|
| UARTx_RTS | UART Data Request To Send | O |
| UARTx_TX | UART Data Transmit | O |
| UARTx_RX | UART Data Receive | I |
| S_UART_TX | UART Data Transmit | O |
| S_UART_RX | UART Data Receive | I |
| TWI (x=[2:0]) | | |
| TWIx_SCK | TWI Serial Clock Signal | I/O |
| TWIx_SDA | TWI Serial Data Signal | I/O |
| S_TWI_SCK | TWI Serial Clock Signal | I/O |
| S_TWI_SDA | TWI Serial Data Signal | I/O |

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5. ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 5-1 Absolute Maximum Ratings

| Symbol | Parameter | MIN | Max | Unit |
|-------------|-------------------------------------|------|------|------|
| $I_{I/O}$ | In/Out current for input and output | -40 | 40 | mA |
| VDD18 | Power Supply for System | -0.3 | 1.98 | V |
| VDD-SYS | Power Supply for System | -0.3 | 1.3 | V |
| VDD-CPUA | Power Supply for CPUA | -0.3 | 1.3 | V |
| VDD-CPUB | Power Supply for CPUB | -0.3 | 1.3 | V |
| VDD-CPUS | Power Supply for CPUS | -0.3 | 1.3 | V |
| VCC-DRAM | Power Supply for DRAM | -0.3 | 1.65 | V |
| VDD-SPLL | Power Supply for DRAM PLL | -0.3 | 1.98 | V |
| VCC33-USB | Power Supply for USB | -0.3 | 3.6 | V |
| VDD09-USB | Power Supply for USB | -0.3 | 1.3 | V |
| VCC12-HSIC | Power Supply for HSIC | -0.3 | 1.32 | V |
| VCC18-HDMI | Power Supply for HDMI | -0.3 | 1.98 | V |
| VDD09-HDMI | Power Supply for HDMI | -0.3 | 1.3 | V |
| VCC18-PLL | Power Supply for system PLL | -0.3 | 1.98 | V |
| VCC18-ADC | Power Supply for HDMI | -0.3 | 1.98 | V |
| VCC18-EFUSE | Power Supply for EFUSE | -0.3 | 1.98 | V |
| VCC18-LDVS | Power Supply for LVDS | -0.3 | 1.98 | V |
| VCC18-MCSI | Power Supply for MIPI-CSI | -0.3 | 1.98 | V |
| VCC18-MDSI | Power Supply for MIPI-DSI | -0.3 | 1.98 | V |
| VCC-IO | Power Supply for Port B | -0.3 | 3.6 | V |
| VCC-PD | Power Supply for Port D | -0.3 | 3.6 | V |
| VCC-PL | Power Supply for Port L | -0.3 | 3.6 | V |
| VDD-GPU | Power Supply for GPU | -0.3 | 1.3 | V |
| T_{STG} | Storage Temperature | -40 | 125 | °C |

5.2. RECOMMENDED OPERATING CONDITIONS

All A83T modules are used under the operating Conditions contained in Table 5-2.

Table 5-2 Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|-------------------------------|------|---------|-------|------|
| Ta | Ambient Operating Temperature | -20 | - | +70 | °C |
| VDD18 | Power Supply for System | 1.62 | 1.8 | 1.98 | V |
| VDD-SYS | Power Supply for System | 0.7 | 0.9 | 1.1 | V |
| VDD-CPUA | Power Supply for CPUA | 0.7 | 0.9 | 1.1 | V |
| VDD-CPUB | Power Supply for CPUB | 0.7 | 0.9 | 1.1 | V |
| VDD-CPUS | Power Supply for CPUS | 0.7 | 0.9 | 1.1 | V |
| VCC-DRAM | Power Supply for DRAM | 1.14 | - | 1.575 | V |
| VDD-SPLL | Power Supply for DRAM | 1.62 | 1.8 | 1.98 | V |
| VCC33-USB | Power Supply for USB | 3.0 | 3.3 | 3.45 | V |
| VDD09-USB | Power Supply for USB | 0.7 | 0.9 | 1.1 | V |
| VCC12-HSIC | Power Supply for HSIC | 1.08 | 1.2 | 1.32 | V |
| VCC18-HDMI | Power Supply for HDMI | 1.62 | 1.8 | 1.98 | V |
| VDD09-HDMI | Power Supply for HDMI | 0.7 | 0.9 | 1.1 | V |
| VCC18-PLL | Power Supply for PLL | 1.62 | 1.8 | 1.98 | V |
| VCC18-ADC | Power Supply for ADC | 1.62 | 1.8 | 1.98 | V |
| VCC18-EFUSE | Power Supply for ADC | 1.62 | 1.8 | 1.98 | V |
| VCC18-LDVS | Power Supply for LVDS | 1.62 | 1.8 | 1.98 | V |
| VCC18-MCSI | Power Supply for MCSI | 1.62 | 1.8 | 1.98 | V |
| VCC18-MDSI | Power Supply for MDSI | 1.62 | 1.8 | 1.98 | V |
| VCC-IO | Power Supply for Port B | 1.7 | 1.8~3.3 | 3.6 | V |
| VCC-PD | Power Supply for Port D | 1.7 | 1.8~3.3 | 3.6 | V |
| VCC-PL | Power Supply for Port L | 1.7 | 1.8~3.3 | 3.6 | V |
| VDD-GPU | Power Supply for GPU | 0.7 | 0.9 | 1.1 | V |

5.3. DC ELECTRICAL CHARACTERISTICS

Table 5-3 summarizes the DC electrical characteristics of A83T.

Table 5-3 DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|----------------------------------|---------|-----|---------|------|
| V _{IH} | High-Level Input Voltage | 0.7*VCC | - | VCC+0.3 | V |
| V _{IL} | Low-Level Input Voltage | -0.3 | - | 0.3*VCC | V |
| R _{PU} | Input pull-up resistance | 50 | 100 | 150 | KΩ |
| R _{PD} | Input pull-down resistance | 50 | 100 | 150 | KΩ |
| I _{IH} | High-Level Input Current | - | - | 10 | uA |
| I _{IL} | Low-Level Input Current | - | - | 10 | uA |
| V _{OH} | High-Level Output Voltage | VCC-0.2 | - | VCC | V |
| V _{OL} | Low-Level Output Voltage | 0 | - | 0.2 | V |
| I _{OZ} | Tri-State Output Leakage Current | -10 | - | 10 | uA |
| C _{IN} | Input Capacitance | - | - | 5 | pF |
| C _{OUT} | Output Capacitance | - | - | 5 | pF |

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, Table 5-4 lists the 24MHz crystal specifications.

Table 5-4 24MHz Oscillator Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|---------------------------------------|-------------|--------|-----|------|
| 1/(t _{CPMAIN}) | Crystal Oscillator Frequency Range | - | 24.000 | - | MHz |
| t _{ST} | Startup Time | - | - | - | ms |
| | Frequency Tolerance at 25 °C | -40 | - | +40 | ppm |
| | Oscillation Mode | Fundamental | | | - |
| | Maximum change over temperature range | -50 | - | +50 | ppm |
| P _{ON} | Drive level | - | - | 50 | uW |
| C _L | Equivalent Load capacitance | - | - | - | pF |
| CL1,CL2 | Internal Load capacitance(CL1=CL2) | - | - | - | pF |
| R _S | Series Resistance(ESR) | - | - | - | Ω |
| | Duty Cycle | 30 | 50 | 70 | % |
| C _M | Motional capacitance | - | - | - | pF |
| C _{SHUT} | Shunt capacitance | - | - | - | pF |
| R _{BIAS} | Internal bias resistor | | | | MΩ |

5.5. POWER ON AND POWER OFF SEQUENCE

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.

Following Figure 5-1 and 5-2 illustrates the power on and off sequence:

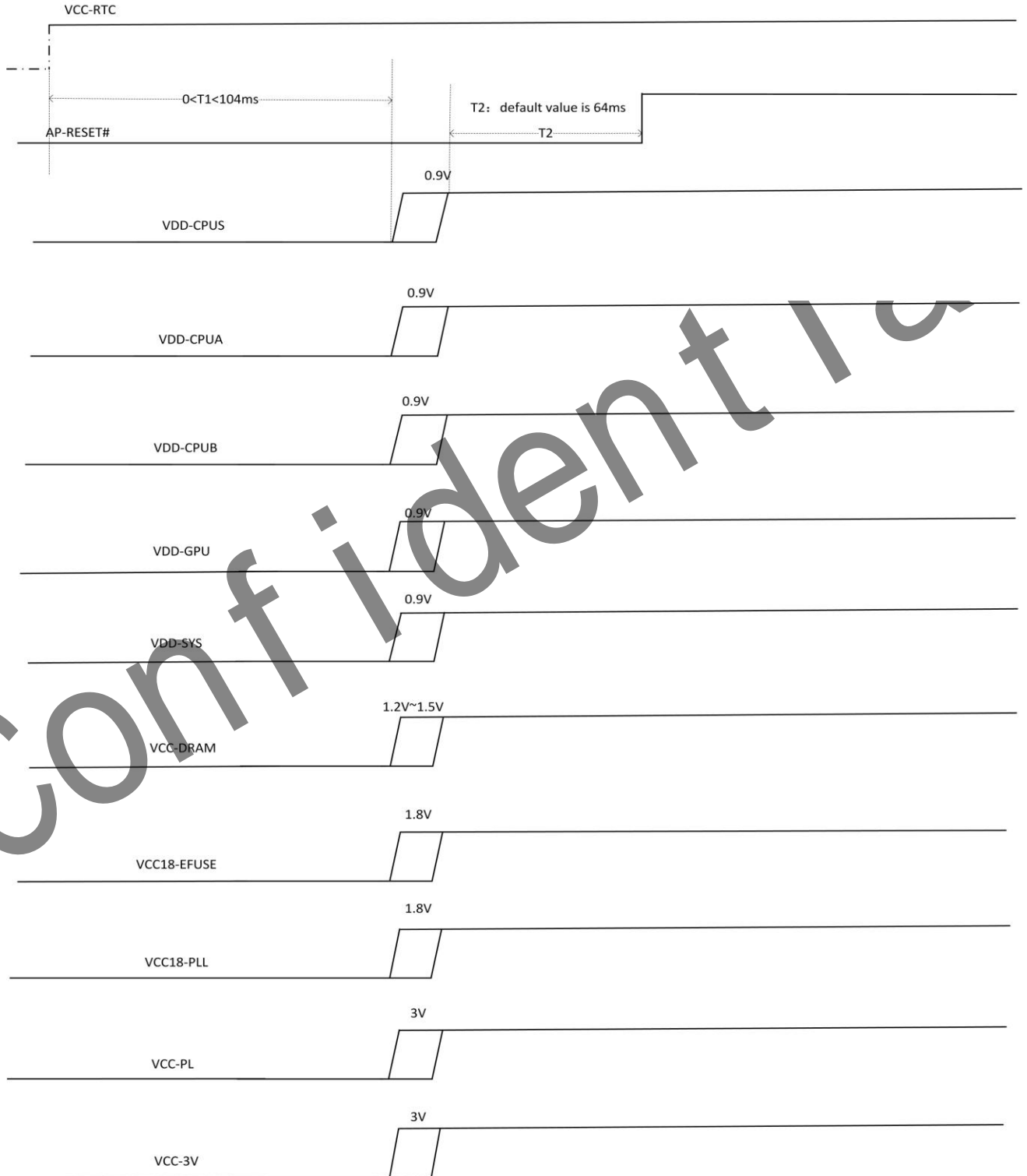


Figure 5-1. Power On Timing

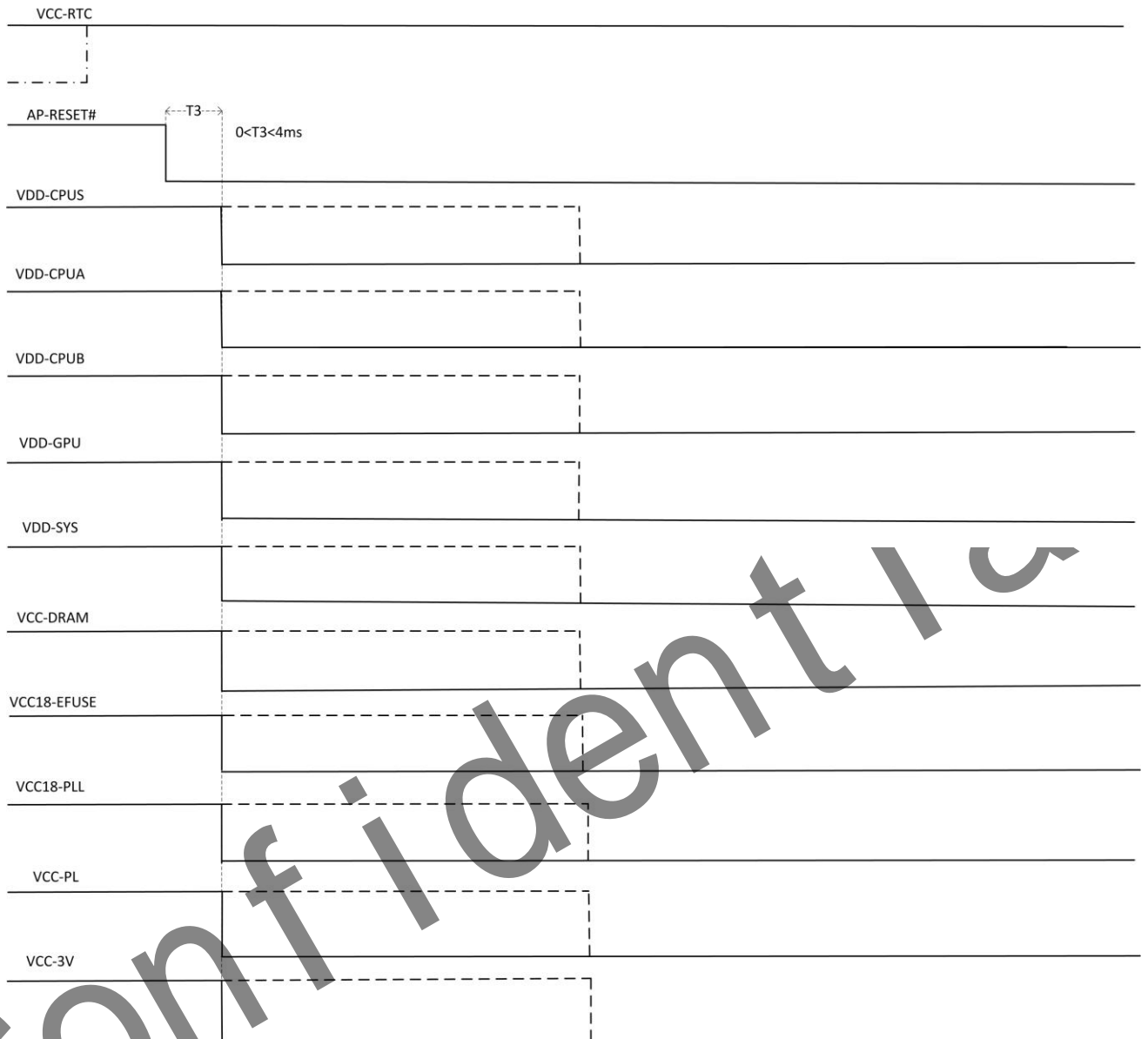


Figure 5-2. Power Down Timing

6. PIN ASSIGNMENT

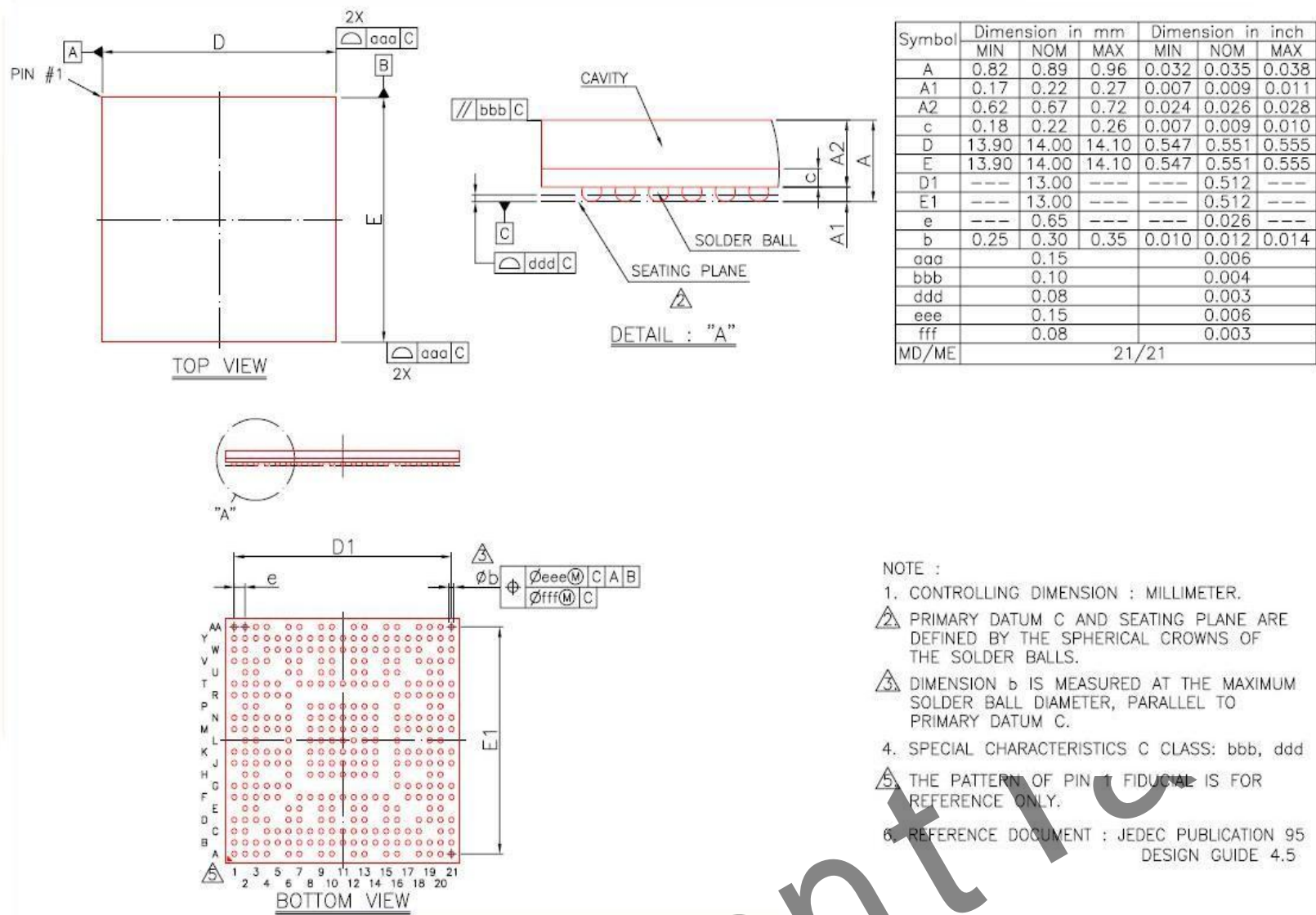
6.1. PIN MAP

The following pin maps show the top views of the 345-pin FBGA package.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | |
|----|-------|--------|-------|-------|---------|----------|----------|-----------|-----------|-------------|-----------|-------------|-------------|------------|-----------|-----------|-----------|----------|-----------|------------|-----------|----|
| A | GND | SDQ20 | SDQ23 | SDQ24 | | SDQS3B | SDQ29 | | PB9 | PB5 | | PE18 | PE16 | | PD18 | PD20 | | PD24 | PD26 | PD2 | GND | A |
| B | SDQ22 | SDQ21 | SDQM3 | SDQ25 | SDQ27 | SDQS3 | SDQ31 | SDQ30 | PB7 | PB3 | PB2 | PE17 | PE15 | PE8 | PD19 | PD21 | PD22 | PD25 | PD27 | PD3 | PD6 | B |
| C | SDQS2 | SDQS2B | | SDQ26 | SRST | SDQ28 | GND | PB8 | PB4 | PE19 | GND | PE14 | PE12 | PE10 | PE3 | PD23 | PD28 | PD29 | | PD7 | PD10 | C |
| D | SDQ18 | SDQ17 | SDQ19 | SRAS | | SADBG | SDDBG1 | | PB10 | PB0 | | PE13 | PE7 | | PE4 | PE2 | | PD4 | PD5 | PD11 | PD12 | D |
| E | | SDQ16 | SODT0 | | | SDDBG0 | VCC-DRAM | | PB6 | PB1 | | PE11 | PE6 | | PE0 | PE1 | | | | PD13 | PD14 | E |
| F | SWE | SCAS | SDQM2 | SODT1 | GND | | VCC-DRAM | VDD18 | VCC-IO | VDD-C PUB | VDD-C PUB | VCC18-LVDS | VCC-PD | VCC-PD | PE5 | | PE9 | PD15 | MDSI-DN3 | MDSI-DP3 | MDSI-DN2 | F |
| G | SBA2 | SBA0 | SA8 | SA9 | SA13 | GND | | | | | | | | | | GND | GND | MDSI-CKN | MDSI-CKP | MDSI-DN1 | MDSI-DP2 | G |
| H | | SA6 | SA7 | | | GND | | GND | VDD-C PUB | VDD-C PUB | VDD-C PUB | GND | VCC18-MDSI | GND | | GND | | | | MDSI-DP1 | MDSI-DN0 | H |
| J | SCK | SCKB | SA5 | SCKE0 | SCKE1 | VCC-DRAM | | GND | VDD-C PUB | VDD-C PUB | VDD-C PUB | VDDFB-C PUB | GND | VDD-SYS | | VDD-SYS | GND | HHPD | MDSI-DP0 | HTX2P | HTX2N | J |
| K | SVREF | SCS0 | SA4 | SCS1 | GND | VCC-DRAM | | GND | GND | GND | GND | GND | VDD09-HDMI | VCC18-HDMI | | VDD-SYS | PG0 | PG1 | HTX0P | HTX1P | HTX1N | K |
| L | | SDQ7 | SA3 | | | VCC-DRAM | | GND | VDD-C PUA | VDD-C PUA | VDD-C PUA | VDD-C PUA | VCC-IO | VDD18 | | GND | | | | PG2 | HTX0N | L |
| M | SDQ4 | SDQ5 | SDQ6 | SA2 | SA1 | VCC-DRAM | | GND | VDD-C PUA | VDDFB-C PUA | VDD-C PUA | VDD-C PUA | VDD-C PUA | VDD-C PUA | VDD-C PUA | PG3 | PG4 | PG5 | PG6 | HTXCP | HTXCN | M |
| N | SDQS0 | SDQS0B | SDQ3 | SA0 | GND | VCC-DRAM | | VDD-SP LL | GND | GND | GND | GND | GND | VCC18-MCSI | GND | PG7 | GND | PG8 | PG9 | PG10 | PG11 | N |
| P | | SDQ2 | SA10 | | | VCC-DRAM | | GND | VDD-G PU | VDD-G PU | VDD-G PU | GND | VDD09-USB | VCC12-HSIC | | GND | | | | PG12 | MCSI-DN3 | P |
| R | SDQ1 | SDQ0 | SDQM0 | SA15 | SA12 | VCC-DRAM | | | | | | | | | | VCC33-USB | VDD-C PUS | PG13 | MCSI-DP3 | MCSI-DP2 | MCSI-DN2 | R |
| T | SDQ15 | SDQ14 | SDQ13 | SBA1 | SZQ | | VCC-IO | VDD18 | PC14 | PC8 | VDD-G PU | VCC18-PLL | VCC18-ADC | GND-ADC | VCC-PL | | VDD-C PUS | GND | MCSI-DN1 | MCSI-CKP | MCSI-CKN | T |
| U | | SDQ12 | SA11 | | | GND | PH8 | | PH0 | PC9 | | X24MI | VCC18-EFUSE | | UBOOT | PL7 | | | | MCSI-DN0 | MCSI-DP1 | U |
| V | SDQS1 | SDQS1B | SDQ11 | SA14 | | PH11 | PH6 | | PC15 | PC10 | | PC1 | X24MO | | PL4 | PL3 | | PL11 | MCSI-DP0 | HSIC-S TRB | HSIC-DATA | V |
| W | SDQ10 | SDQ9 | | PF3 | JTAGSEL | PH10 | PH5 | PH1 | PC16 | PC11 | PC6 | PC3 | REXT | PL1 | LRADC0 | PL2 | PL5 | PL10 | | USB0-DM | USB0-DP | W |
| Y | SDQ8 | SDQM1 | PF5 | PF1 | PF0 | PH9 | PH4 | PH2 | PC17 | PC12 | PC7 | PC4 | PC0 | TEST | RTC-VIO | NMI | PL6 | PL9 | USB0-VBUS | USB1-DP | USB0-ID | Y |
| AA | GND | PF6 | PF4 | PF2 | | PH7 | PH3 | | PC18 | PC13 | | PC5 | PC2 | | PL0 | RESET | | PL8 | PL12 | USB1-DM | GND | AA |

6.2. PACKAGE DIMENSION

The following diagram shows the package dimension of the A83T.



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