MYD-YT507H
EVK Hardware User Guide

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History

Version	Author	Participants	Date	Description
V1.0	Dana		20220410	Initial Version

Contents

1. Overview

In response to industry applications and customer demand for high performance board cards, MYIR Electronics has launched a development kit based on the T507-H processor: MYD-YT507H.The development board is composed of a core board MYC-YT507H and a carrier board MYB-YT507H.

The core board supports 100M,1000M Ethernet, HDMI, LVDS, MIPI-CSI, USB2.0, TWI, I2S, ADC, Line-out, CVS-out and other common communication and multimedia interfaces.We provide complete software packages with accompanying documentation to help customers reduce development difficulties, speed up product development and shorten time to market. In the development stage, it is suggested to speed up the development with the evaluation kit MYD-YT507H matching the core board.

1.1. EVK Introduction

MYC-YT507H core board uses Allwinner T5 series processor as the main control platform, on board power management chip, single LPDDR4, eMMC.The core board and carrier board are welded with stamp holes, which helps to reduce costs and ensure the stability of the connection between the core board and the carrier board .

MYB-YT507H is an extended carrier board used with MYC-YT507H core board, with 12V 2A DC power supply. Equipped with one 4G PCIE interface, one digital DVP camera input, one MIPI CSI, two LVDS display interface (single/dual channel support), one Gigabit Ethernet interface, one hundred Gigabit Ethernet, one TV display output, headset output, SPDIF audio output, two USB HOST Type A, USB Type-C DRP, Micro SD, HDMI, raspberry PI and other peripheral interfaces.

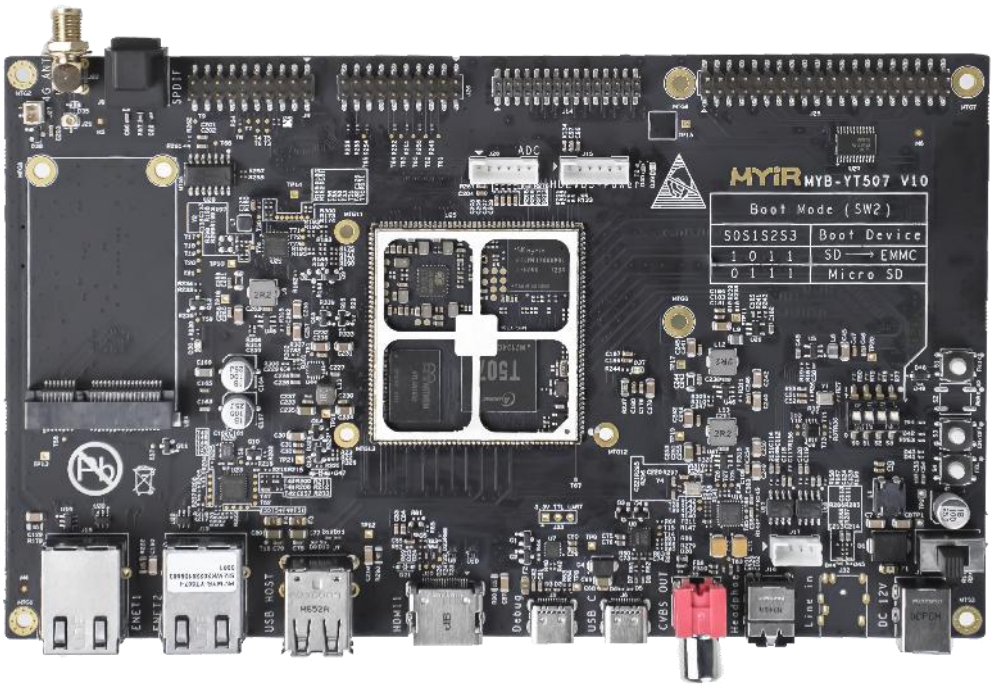

Figure 1- 1 MYD-YT507H Kit

1.2. Block Diagram

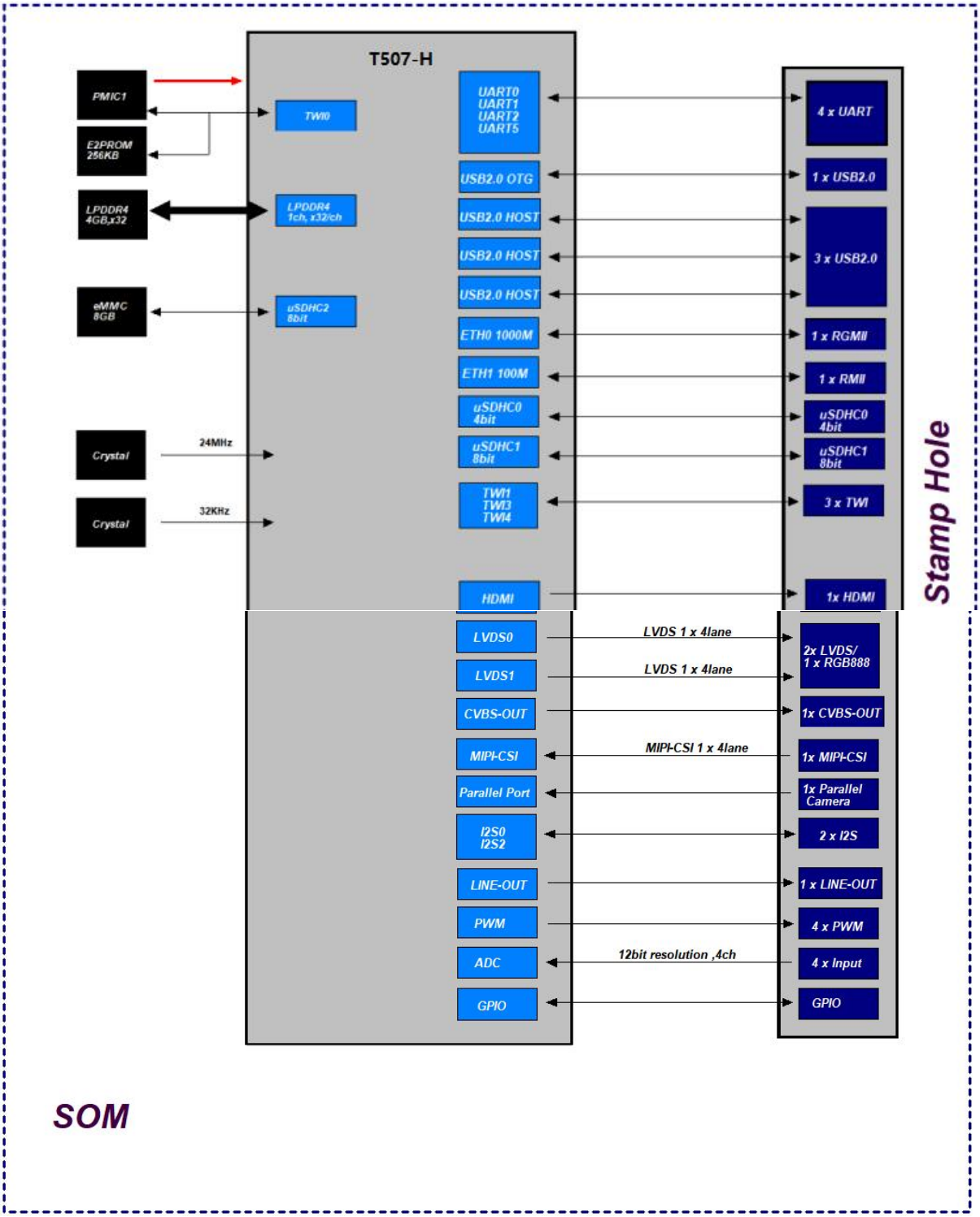

Figure 1- 2 core board diagram

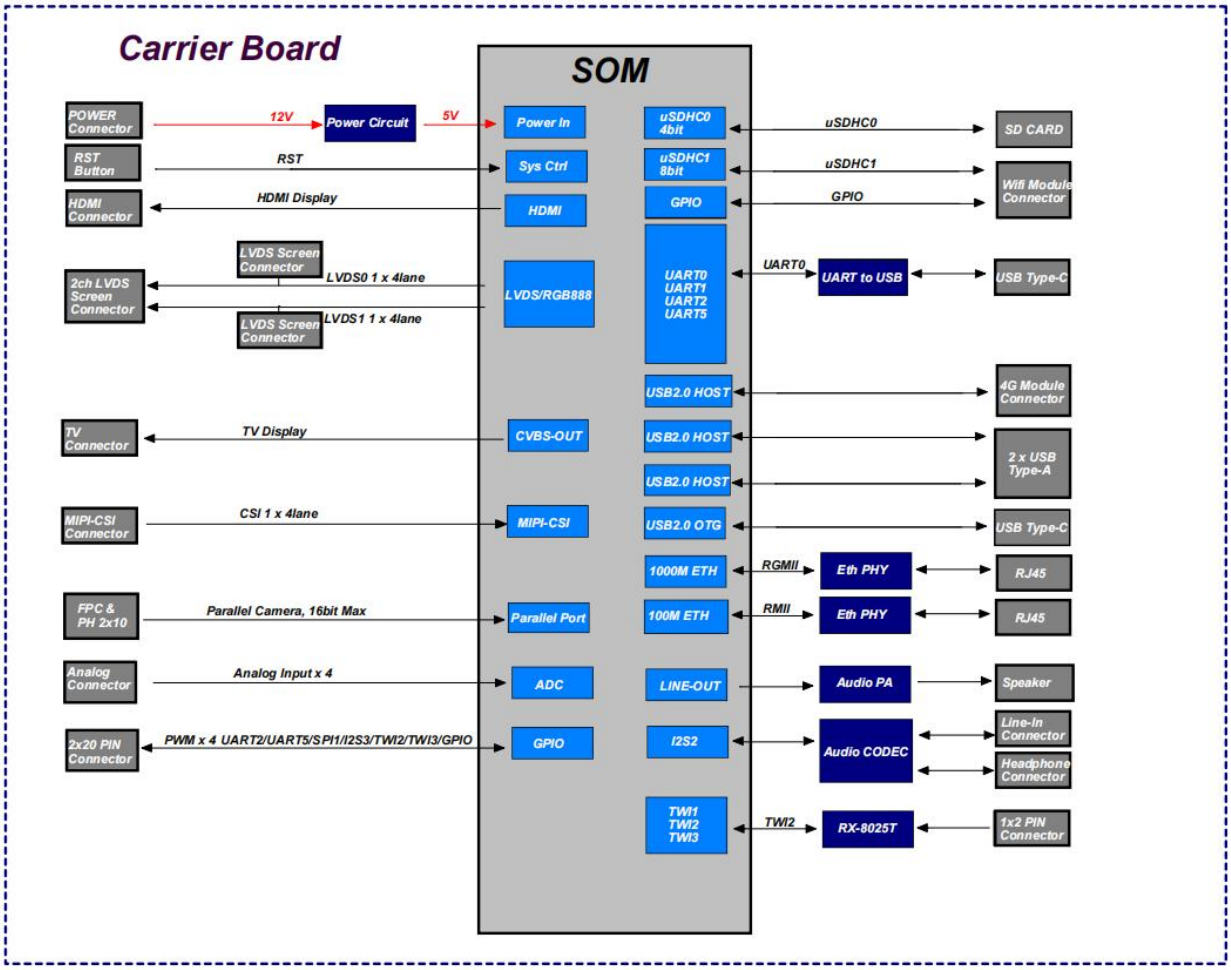

Figure 1- 3 carrier board diagram

1.3. EVK Physical Image

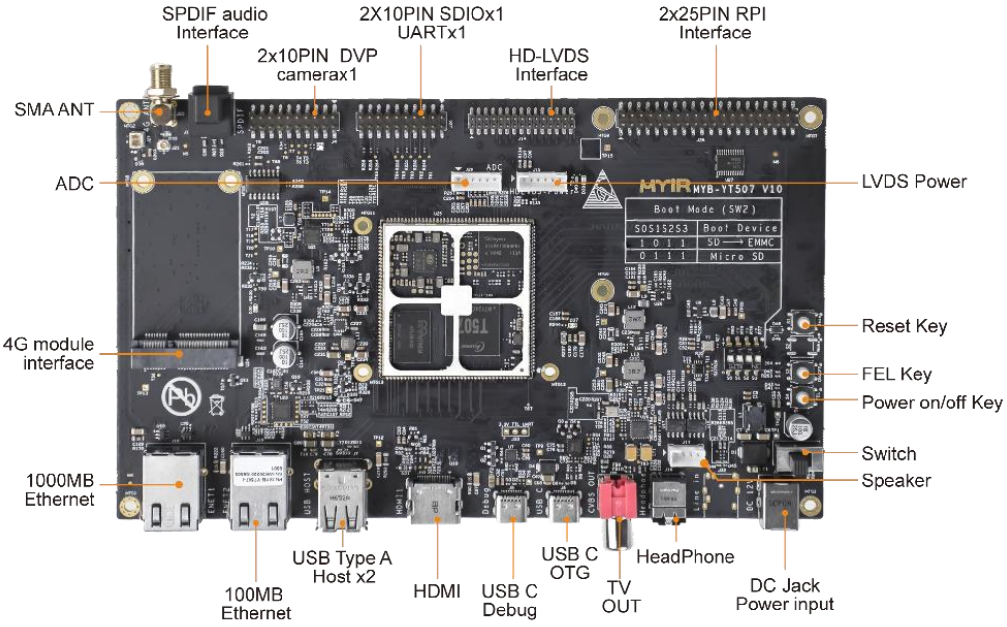

Figure 1- 4 MYB-YT507H Top view of EVK

Figure 1-5 MYB-YT507H Bottom view of EVK

1.4. Reference Resource

MYIR Electronics provides development resource, including but not limited to the product manua l, hardware design guide, device manual, software development guide, system mirror image, etc. Please go to http://d.myirtech.com/MYD-YT507H/ for download.

2. Power Parameters

2.1. Power Tree

The input voltage of the system is 12V, which is converted into an appropriate voltage for core board and carrier board peripherals by DCDC chip. The converted voltage mainly includes 5V/3.6V/3.3V/1.8V, etc.

The carrier board and core board are powered separately. One DC-DC output 5V mainly supplies power to the core board, and the other DC-DC output 5V supplies power to carrier board peripherals such as HDMI, USB HOST, USB OTG, Audio Amplify, and LVDS. The 3.6V voltage mainly supplies power to 4G modules; 3.3V voltage mainly supplies power to PHY and Audio of the base plate; The 1.8V voltage mainly supplies power to the MIPI-CSI interface. The power supply topology is as follows:

The RTC battery input is an optional power input. When the system is powered off and the RTC does not need to work, do not provide this power input.

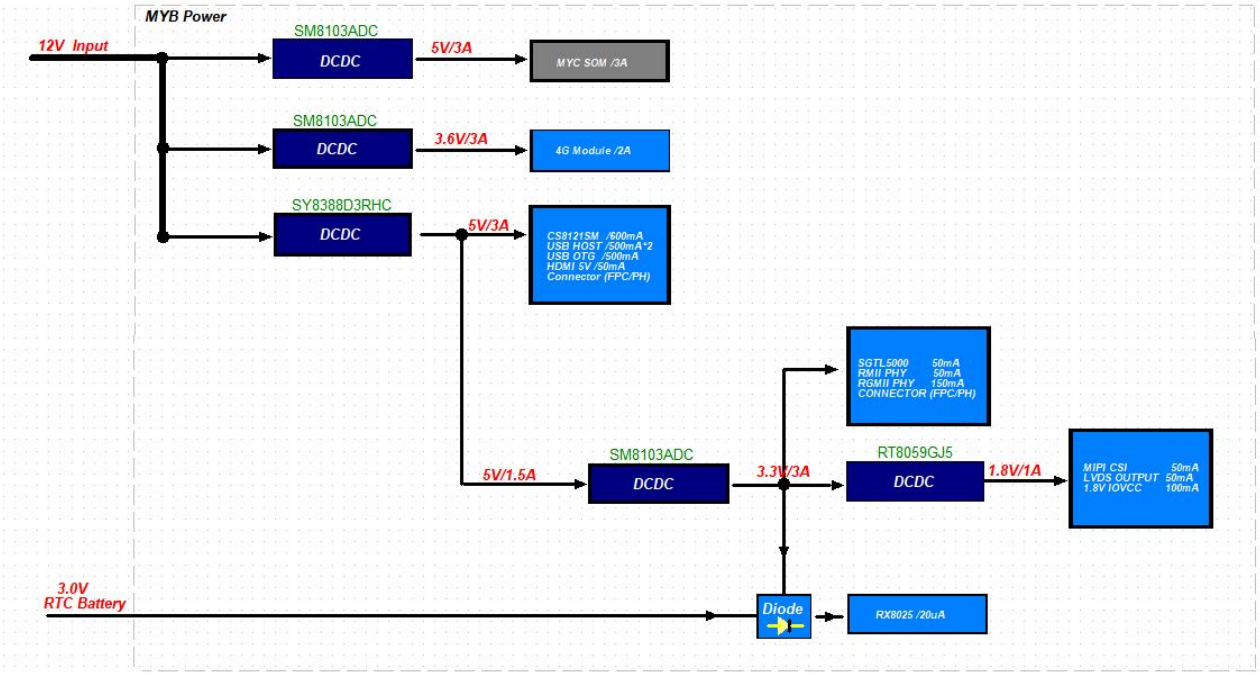

Figure 2 - 1 EVK Power Tree

2.2. Power Consumption

Condition	Voltage	Current	Power Consumption
Mem state command：echo mem> /sys/power/state	12.0V	0.03A	0.36W
Freeze state command：echo freeze> /sys/power/state	12.0V	0.06A	0.72W
In the linux environment No peripherals	12.0V	0.1A	1.2W
In the linux environment Peripherals fully loaded（USB x2，PHY x2，raspberry PI，HDMI，CSI）	12.0V	0.35A	4.2W

Table 2 - 1 EVK Power Consumption

2.3. Requirement of Power Supply

The carrier board standard supply voltage is 12V. If the customer does not want to use 12V power supply, the supply voltage can also be adjusted within 6-18V wide voltage range.Note that if the user uses a non-12V input power supply but satisfies the wide range of power supply, it is necessary to ensure that the power supply capacity is sufficient.

3. Boot Configure

T507-H will sample the BOOT SEL pin at the rising edge of CPU reset signal, and decide to start the device according to the level of the BOOT SEL pin.

3.1. Boot Device

After a power-on reset, the T507-H processor starts up by executing the program in the chip's internal BROM. BROM starts by reading the voltage level of the pin of BOOT SEL[4:0], and the levels of different combinations will enter the specific starting source.

BOOT SEL[4:0] pins do not add pull-up or pull-down design in the core plate. But there is a 15K pull-up resistor inside the chip by default. MYC-YT507H core board start up mode mainly has eMMC start up, Micro SD card start up. See Table 3-1.

BOOT SEL[4:0]	Initial Boot Source	instructions
11101	Micro SD -> eMMC	Boot from Micro SD card first, eMMC second
11111	Micro SD	Can only boot from Micro SD card

Table 3 - 1 Boot device configuration

4. Interface Layout

The overall interface layout map of the evaluation board is as follows.

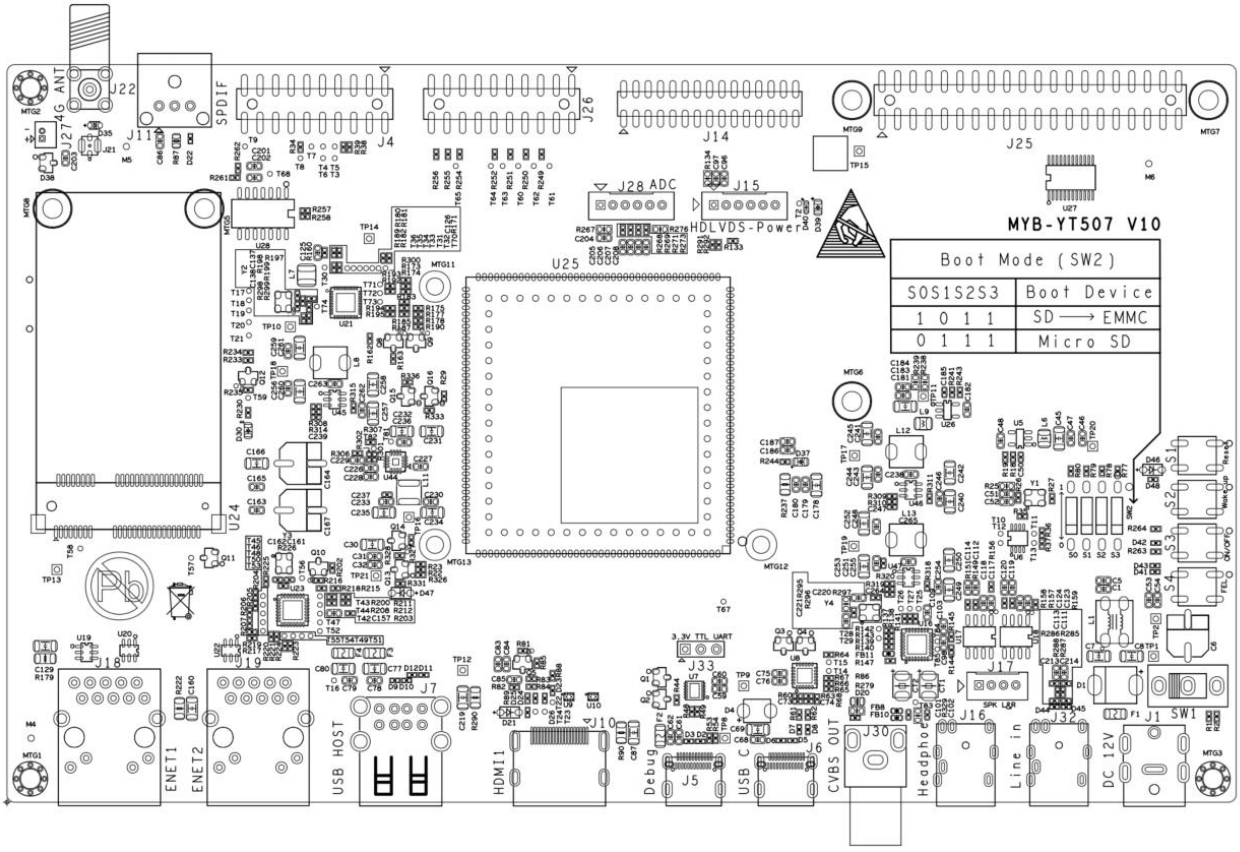

Figure 4 - 1 MYD-YT507H Interface Layout

4.1. Power Interface

The power input connector is DC Jack.Evaluation board power supply has no over voltage protection, please use the specified operating voltage.

It is recommended to use the 12V 2A DC adapter as the power input, the non-12V DC adapter please refer to the Section 2.3 power consumption and power supply requirements to choose the appropriate power supply.

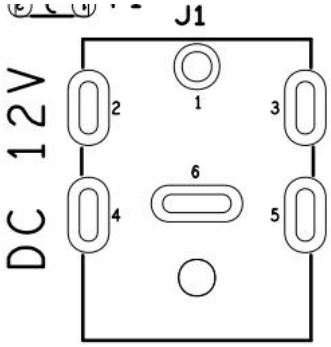

Figure 4 - 3 Connector of Power Input

4.1.1. Pin Description

Ref	Pin	Function	Name	Comments
J1	1	System power input, positive pole	12V	DC Jack, recommended DC heads external diameter is 5.6mm, and inner diameter is 1.65mm
	2	NC	NC	
	3	NC	NC	
	4	NC	NC	
	5	NC	NC	
	6	GND	GND	

Table 4 - 1 Power interface description

4.2. Debug

System debugging serial port uses UART2. MYD-YT507H converts UART to USB signal through serial port to USB chip. During debugging, USB cable only needs to be connected to TYPE C interface of J5.

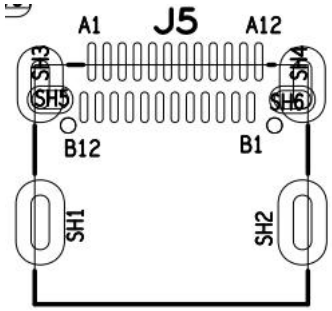

Figure 4 - 4 Debug

4.2.1. Pin Description

Ref	Pin	Function	Name	Comments
J5	A4	USB 5V power supply	USB_TC2_VBUS	
	A9	USB 5V power supply	USB_TC2_VBUS	
	B9	USB 5V power supply	USB_TC2_VBUS	
	B4	USB 5V power supply	USB_TC2_VBUS	
	A6	USB data+	USB_DP_Debug	
	A7	USB data-	USB_DN_Debug	
	B6	USB data+	USB_DP_Debug	
	B7	USB data-	USB_DN_Debug	
	A2	NC	NC	
	A3	NC	NC	
	B11	NC	NC	
	B10	NC	NC	
	B2	NC	NC	
	B3	NC	NC	
	A11	NC	NC	
	A10	NC	NC	
	A5	NC	GND	
	B5	NC	GND	
	A8	NC	NC	
	B8	NC	NC	
	A1	GND	GND	

	A12	GND	GND	
	B12	GND	GND	
	B1	GND	GND	

Table 4-2 Debug port

4.3. Key

The evaluation board is designed with three buttons. They are ON/OFF button, reset button and FEL button.

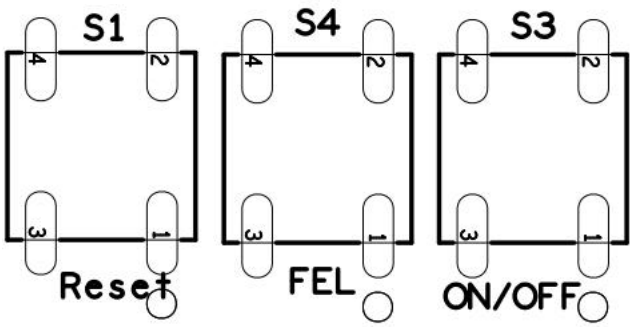

Figure 4-5 KEY

4.3.1. Pin Description

Ref	Pin	Function	Name	Comments
S1	Reset	Reset button	CPU-RESET	Key pressing produces a reset
S3	ONOFF	Power on, power off	CPU-ONOFF	Button can turn on, turn off
S4	FEL	Flash button	FEL	Press the flash

Table 4-3 Key description

4.4. LED

The evaluation board is designed with 4 LED lights. D37 LED is on core board used as running indicator light, lit in red, on behalf of CPU normal operation; Other three leds is on carrier board.

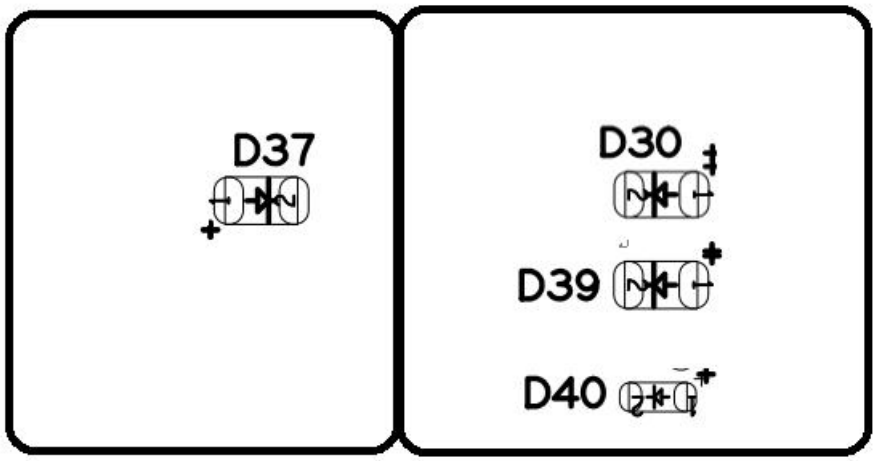

Figure 4 - 6 LED

4.4.1. Pin Description

Ref	Pin	Function	Name	Comments
D37	PWR	Core board running indicator light, red	/	On: The device is working properly
D39	PWR	Bottom panel running indicator, red	/	Off: The device is powered off
D30	RUN	LTE signal indicator, red	/	On: The device is working properly
D40	User	User-defined IO in blue	NCSI0-D15	Off: The device is powered off

Table 4-4 LED description

4.5. SD Card

The evaluation board designs a Micro SD card circuit, which Can be use as boot device or storage device When a card is inserted.

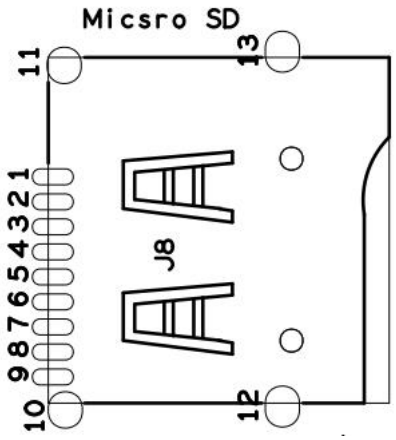

Figure 4-7 Micro SD

4.5.1. Pin Description

Ref	Pin	Function	Name	Comments
J8	1	Data 2	SDIO0-D2	
	2	Data 3	SDIO0-D3	
	3	command	SDIO0-CMD	
	4	3.3V Power supply	VSOM-3V3	
	5	clock	SDIO0-CLK	
	6	GND	GND	
	7	Data 0	SDIO0-D0	
	8	Data 1	SDIO0-D1	
	9	Card detection	SDIO0-DET	
	10	GND	GND	
	11	GND	GND	
	12	GND	GND	
	13	GND	GND	

Table 4-5 Micro SD pin description

4.6. GPIO/TWI/UART

MYB-YT507H provides a 40 pin 2.54mm pitch double row connector and J25 interface. Through TWI interface, PCF8575 chip is used to provide universal remote I/O expansion for the EVK. All idle GPIO/TWI/UART have been drawn out, convenient for users to connect with other devices.

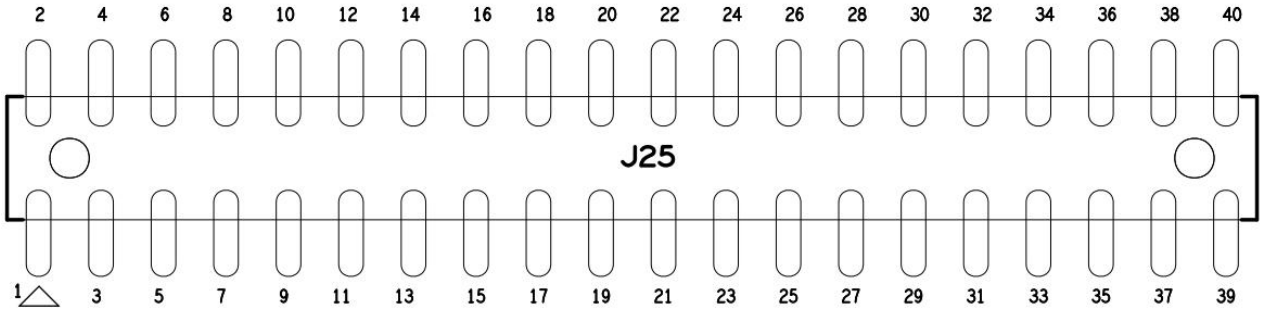

Figure 4 - 8 GPIO/TWI/UART Expand Connector

4.6.1. Pin Description

Ref	Pin	Function	Name	Comments
J25	1	power 3.3V	VDD_3V3	
	2	power 5V	VDD_5V	
	3	I2C bus data	TWI4-SDA	
	4	output power 5V	VDD_5V	
	5	I2C bus clock	TWI4-SCK	
	6	GND	GND	
	7	General GPIO	NCSI0-D11	
	8	UART Send	UART2-TX	
	9	GND	GND	
	10	UART Receive	UART2-RX	
	11	General GPIO	P17	
	12	General GPIO	P00	
	13	General GPIO	P16	
	14	GND	GND	
	15	General GPIO	P15	
	16	General GPIO	P07	
	17	output power 3.3V	VDD_3V3	
	18	General GPIO	P10	
	19	General GPIO	PD26	
	20	GND	GND	

	21	General GPIO	PD21	
	22	General GPIO	P01	
	23	NC	NC	
	24	General GPIO	P02	
	25	GND	GND	
	26	General GPIO	P03	
	27	I2C bus data	TWI3-SDA	
	28	I2C bus clock	TWI3-SCK	
	29	General GPIO	P14	
	30	GND	GND	
	31	General GPIO	P13	
	32	General GPIO	P04	
	33	General GPIO	P12	
	34	GND	GND	
	35	General GPIO	P11	
	36	General GPIO	P05	
	37	UART Send	UART5-TX	
	38	General GPIO	P06	
	39	GND	GND	
	40	UART Receive	UART5-RX	

Table 4- 6 dual-row connector pin description

4.7. USB

The core board leads to three USB 2.0 HOST interfaces (USB1, USB2, USB3) and one USB 2.0 OTG interface (USB0).

Evaluation board USB0 supports OTG/DRP mode, with USB 2.0 OTG Type-C interface, J6; Evaluation board USB1 and USB3 support HOST mode, with USB 2.0 HOST Type-A interface, J7. In addition, one USB2 communicates with the 4G module. Please refer to the 4G module introduction for details.

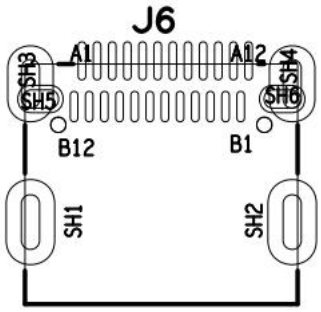

Figure 4 - 9 USB Type-C connector

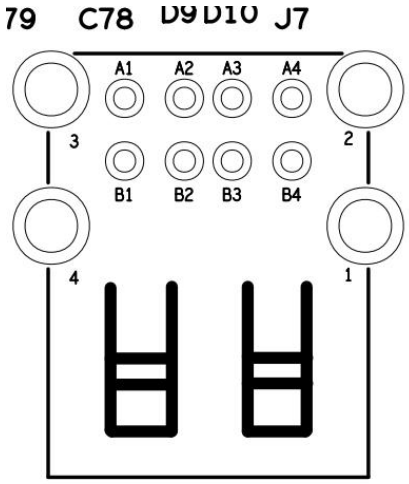

Figure 4 - 10 USB HOST connector

4.7.1. Pin Description

Ref	Pin	Function	Name	Comments
	A4	USB 5V power supply	USB_TC1_VBUS	
	A9	USB 5V power supply	USB_TC1_VBUS	
	B9	USB 5V power supply	USB_TC1_VBUS	
	B4	USB 5V power supply	USB_TC1_VBUS	
	A6	USB data+	USB0-DP	
	A7	USB data-	USB0-DN	

J6	B6	USB data+	USB0-DP	
	B7	USB data-	USB0-DN	
	A2	USB transmit data+	NC	
	A3	USB transmit data-	NC	
	B11	USB receive data+	NC	
	B10	USB receive data-	NC	
	B2	USB transmit data+	NC	
	B3	USB transmit data-	NC	
	A11	USB receive data+	NC	
	A10	USB receive data-	NC	
	A5	TYPE-C CC1	USB2CC1	
	B5	TYPE-C CC2	USB2CC2	
	A8	NC	NC	
	B8	NC	NC	
	A1	GND	GND	
	A12	GND	GND	
	B12	GND	GND	
	B1	GND	GND	

表 4 - 7 USB OTG/DRP pin description

位号	标识	功能	信号	说明
J7	A1	USB 5V power supply	VCC5V	
	A2	USB1 HOST data -	HOST1_USB_DM	
	A3	USB1 HOST data +	HOST1_USB_DP	
	A4	GND	GND	
	B1	USB 5V power supply	VCC5V	
	B2	USB2 HOST data -	HOST2_USB_DM	
	B3	USB2 HOST data +	HOST2_USB_DP	
	B4	GND	GND	
	1	Metal GND	GND_EARTH	
	2	Metal GND	GND_EARTH	
	3	Metal GND	GND_EARTH	
	4	Metal GND	GND_EARTH	

Table 4 - 8 USB HOST pin description

4.8. Ethernet

The core board leads to two Ethernet communication interfaces. The RGMII communication interface leads to the integrated network transformer integrated RJ45 connector through the YT8511 PHY chip, providing gigabit network port J18. The RMII communication interface passes through the YT8512 PHY chip and leads to the integrated RJ45 connector for the integrated network transformer, providing 100 M bit/s network port J19.

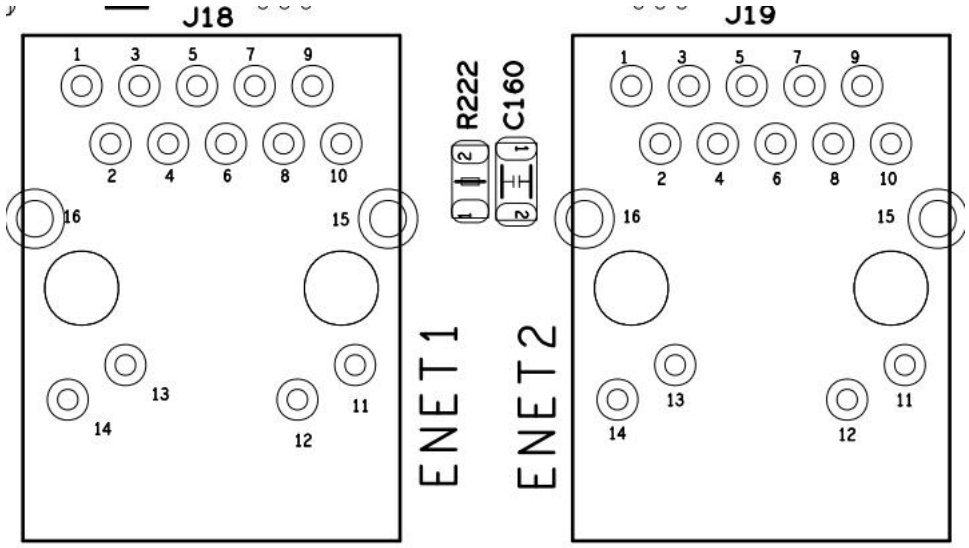

Figure 4-11 Ethernet connector

4.8.1. Pin Description

Ref	Pin	Function	Name	Comments
J18	1	RGMII differential signal 0+	MDI1_TRX_D0P	
	2	RGMII differential signal 0-	MDI1_TRX_D0N	
	3	RGMII differential signal 1+	MDI1_TRX_D1P	
	4	RGMII differential signal 1-	MDI1_TRX_D1N	
	5	GND	GND	
	6	GND	GND	
	7	RGMII differential signal 2+	MDI1_TRX_D2P	
	8	RGMII differential signal 2-	MDI1_TRX_D2N	
	9	RGMII differential signal 3+	MDI1_TRX_D3P	
	10	RGMII differential signal 3-	MDI1_TRX_D3N	
	11	LINK LED	LED_ACT1	
	12	GND	GND	
	13	ACTIVITY LED	ETH_LED1	
	14	GND	GND	

	15	Shield GND	GND_EARTH	
	16	Shield GND	GND_EARTH	
J19	1	RMII differential signal 0 +	MDI2_TRX_D0P	
	2	RMII differential signal 0 -	MDI2_TRX_D0N	
	3	RMII differential signal 1 +	MDI2_TRX_D1P	
	4	RMII differential signal 1 -	MDI2_TRX_D1N	
	5	GND	GND	
	6	GND	GND	
	7	NC	NC	
	8	NC	NC	
	9	NC	NC	
	10	NC	NC	
	11	Power 3.3 V	VDD_3V3	
	12	LINK LED	LED_RMII_100M	
	13	NC	NC	
	14	NC	NC	
	15	Shield GND	GND_EARTH	
	16	Shield GND	GND_EARTH	

Table 4-9 Ethernet pin description

4.9. CSI

The T507-H processor supports one 4-Lane MIPI-CSI interface and one 16-bit Bus Parallel CSI interface.

The camera adopted by MIPI-CSI interface is a 26-pin 0.5mm FPC row with interface J2. Users can choose the MY-CAM003M camera module of MYIR Technology. Please visit http://www.myir-tech.com/product/my_cam003m.htm for details on this module.

Parallel CSI interface adopts a 30-PIN 0.5mm FPC row with J3 interface. Users can choose the MY-CAM011B camera module of MYIR Technology. Please visit http://www.myir-tech.com/product/my_cam011b.htm for details on this module. At the same time, the Parallel CSI is led out of interface J4 by row pin from the carried plate.

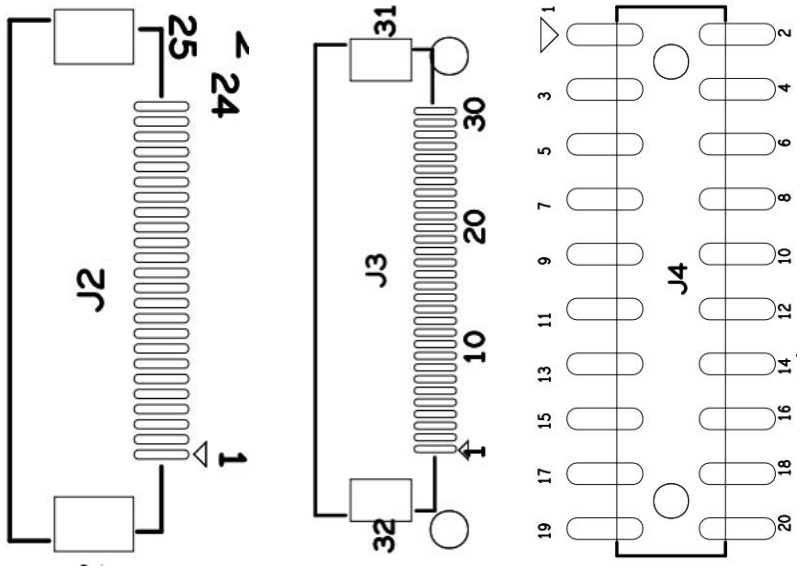

Figure 4-12 MIPI-CSI connector

4.9.1. Pin Description

Ref	Pin	Function	Name	Comments
J2	1	Power 5V	VDD_5V	
	2	CSI Power control	PC7	CAM_EN
	3	NC	NC	
	4	CSI data transmit	MCSI-SDA_1V8	
	5	CSI clock	MCSI-SCL_1V8	
	6	CSI reset signal	PC12	CAM_RST
	7	CSI Enable control	PC2	CAM_PWDN
	8	GND	GND	
	9	CSI master clock	CAM_P1_MCLK	
	10	GND	GND	
	11	MIPI-CSI lane 3+	MCSI-D3P-R	

	12	MIPI-CSI lane 3-	MCSI-D3N-R	
	13	GND	GND	
	14	MIPI-CSI lane 2+	MCSI-D2P-R	
	15	MIPI-CSI lane 2-	MCSI-D2N-R	
	16	GND	GND	
	17	MIPI-CSI clock+	MCSI-CLKP-R	
	18	MIPI-CSI clock-	MCSI-CLKN-R	
	19	GND	GND	
	20	MIPI-CSI lane 1+	MCSI-D1P-R	
	21	MIPI-CSI lane 1-	MCSI-D1N-R	
	22	GND	GND	
	23	MIPI-CSI lane 0+	MCSI-D0P-R	
	24	MIPI-CSI lane 0-	MCSI-D0N-R	

Table 4 - 10 CSI pin description

Ref	Pin	Function	Name	Comments
J3	1	Power 5V	VDD_5V	
	2	Power 3.3V	VDD_3V3IO	
	3	Power 3.3V	VDD_3V3IO	
	4	GND	GND	
	5	CSI control data	NCSI-SDA	
	6	CSI control clock	NCSI-SCK	
	7	CSI reset signal	NCSI_CAM_RST	
	8	CSI Enable control	NCSI_CAM_PD	
	9	GND	GND	
	10	CSI field synchronization signal	NCSI0-VSYNC	
	11	CSI line synchronizes signal	NCSI0-HSYNC	
	12	CSI data 7	NCSI0-D7	
	13	GND	GND	
	14	CSI ref clock	NCSI0-MCLK	
	15	GND	GND	
	16	CSI data 6	NCSI0-D6	
	17	CSI data 5	NCSI0-D5	
	18	GND	GND	
	19	CSI pixel clock	NCSI0-PCLK	
	20	GND	GND	

	21	CSI data 4	NCSI0-D4	
	22	CSI data 0	NCSI0-D0	
	23	CSI data 3	NCSI0-D3	
	24	CSI data 1	NCSI0-D1	
	25	CSI data 2	NCSI0-D2	
	26	NC	NC	
	27	NC	NC	
	28	NC	NC	
	29	NC	NC	
	30	NC	NC	
	31	GND	GND	
	32	GND	GND	

Table 4-11 Parallel CSI pin description

Ref	Pin	Function	Name	Comments
J4	1	Power 5V	VDD_5V	
	2	GND	GND	
	3	Power 3.3V	VDD_3V3IO	
	4	CSI reset signal	NCSI_CAM_RST	
	5	CSI data transmission	TWI3-SDA	
	6	CSI enable control	NCSI_CAM_PD	
	7	CSI clock	TWI3-SCK	
	8	CSI data 7	C_D7	
	9	CSI field synchronization signal	C_VC	
	10	CSI data 6	C_D6	
	11	CSI line synchronizes signal	C_HC	
	12	CSI data 5	C_D5	
	13	CSI pixel clock	C_CLK	
	14	GND	GND	
	15	GND	GND	
	16	CSI data 3	C_D3	
	17	CSI data 4	C_D4	
	18	CSI data 1	C_D1	
	19	CSI data 0	C_D0	
	20	CSI data 2	C_D2	

Table 4-12 dual-row pin Description

4.10. LVDS

T507-H series processors support single/dual LVDS signals, leading three LVDS signal interfaces on the baseboard, LVDS0: X4 Lane, LVDS1:x4 Lane, J12, J13 and J14.

J12 and J13 interfaces are used to connect single LVDS small screen, and FPC module is elicited. J14 interface is used to connect dual LVDS large screen, LVDS1+LVDS0 output at the same time, row pin leads; The single-channel small screen and dual-channel large screen cannot be used at the same time. Customers can choose them based on their own requirements.

By default, J12 and J13 interfaces support 1280 x800 resolution (10.1 inch capacitive screen) driver; The J14 interface supports a 1920x1080 resolution (21.5-inch screen) by default.

In addition, when we use single-channel LVDS1 small screen J13 interface, we should also use J15 interface, J15 is the backlight interface of external screen, using 6pin 2.0mm spacing public seat; The single-channel LVDS0 small screen backlight interface is not designed.

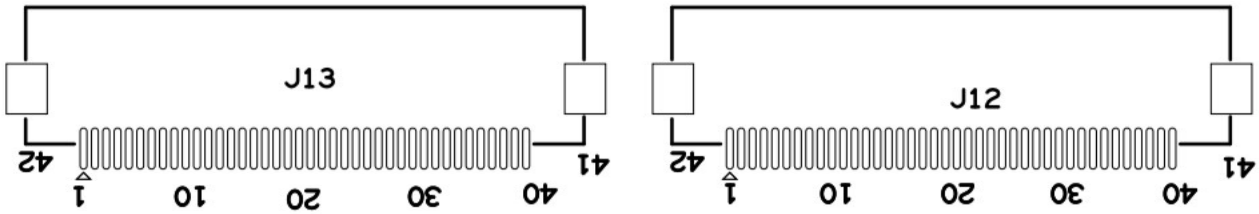

Figure 4-13 Single LVDS port

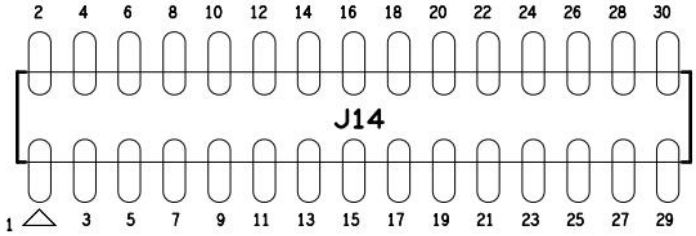

Figure 4-14 Dual LVDS ports

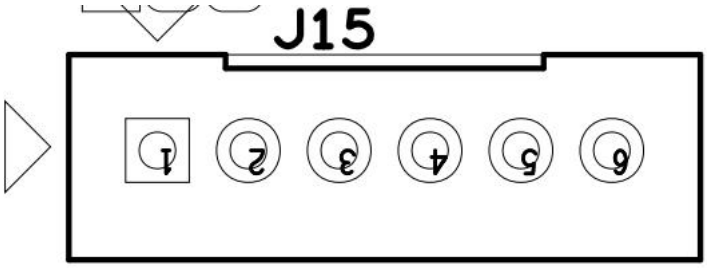

Figure 4-15 LVDS1 backlight interface

4.10.1. Pin Description

Ref	Pin	Function	Name	Comments
	1	NC	NC	
	2	Power 5V	VDD_5V	input
	3	Power 5V	VDD_5V	input

J12	4	NC	NC	
	5	NC	NC	
	6	NC	NC	
	7	GND	GND	
	8	LVDS0 interface data 0 signal-	LVDS0-D0N-R	
	9	LVDS0 interface data 0 signal+	LVDS0-D0P-R	
	10	GND	GND	
	11	LVDS0 interface data 1 signal-	LVDS0-D1N-R	
	12	LVDS0 interface data 1 signal+	LVDS0-D1P-R	
	13	GND	GND	
	14	LVDS0 interface data 2 signal-	LVDS0-D2N-R	
	15	LVDS0 interface data 2 signal+	LVDS0-D2P-R	
	16	GND	GND	
	17	LVDS0 interface clock signal-	LVDS0-CLKN-R	
	18	LVDS0 interface clock signal+	LVDS0-CLKP-R	
	19	GND	GND	
	20	LVDS0 interface data 3 signal-	LVDS0-D3N-R	
	21	LVDS0 interface data 3 signal+	LVDS0-D3P-R	
	22	GND	GND	
	23	NC	NC	
	24	NC	NC	
	25	GND	GND	
	26	NC	NC	
	27	LCD backlight adjustment	PD28	
	28	General GPIO1_IO12	PD27	
	29	NC	NC	
	30	GND	GND	
	31	NC	NC	
	32	NC	NC	
	33	TWI4 bus data transmission	TWI4-SDA	
	34	TWI4 bus clock	TWI4-SCK	
	35	NC	NC	
	36	Interruption of touch screen	PD24	
	37	NC	NC	
	38	NC	NC	
	39	NC	NC	
	40	NC	NC	

	41	GND	GND	
	42	GND	GND	

Table 4-13 single LVDS0 port

Ref	Pin	Function	Name	Comments
J13	1	NC	NC	
	2	Power 5V	VDD_5V	
	3	Power 5V	VDD_5V	
	4	NC	NC	
	5	NC	NC	
	6	NC	NC	
	7	GND	GND	
	8	LVDS1 interface data 0 signal-	LVDS1-D0N-R	
	9	LVDS1 interface data 0 signal+	LVDS1-D0P-R	
	10	GND	GND	
	11	LVDS1 interface data 1 signal-	LVDS1-D1N-R	
	12	LVDS0 interface data 1 signal+	LVDS1-D1P-R	
	13	GND	GND	
	14	LVDS1 interface data 2 signal-	LVDS1-D2N-R	
	15	LVDS1 interface data 2 signal+	LVDS1-D2P-R	
	16	GND	GND	
	17	LVDS1 interface clock signal-	LVDS1-CLKN-R	
	18	LVDS1 interface clock signal+	LVDS1-CLKP-R	
	19	GND	GND	
	20	LVDS1 interface data 3 signal-	LVDS1-D3N-R	
	21	LVDS1 interface data 3 signal+	LVDS1-D3P-R	
	22	GND	GND	
	23	NC	NC	
	24	NC	NC	
	25	GND	GND	
	26	NC	NC	
	27	LCD backlight adjustment	PWM5	
	28	General GPIO1_IO23	PD23	
	29	NC	NC	
	30	GND	GND	
	31	NC	NC	

	32	NC	NC	
	33	TWI3 bus data transmission	TWI3-SDA	
	34	TWI3 bus clock	TWI3-SCK	
	35	NC	NC	
	36	Interruption of touch screen	PD20	
	37	NC	NC	
	38	NC	NC	
	39	NC	NC	
	40	NC	NC	
	41	GND	GND	
	42	GND	GND	

Table 4-14 single LVDS1 port

Ref	Pin	Function	Name	Comments
J14	1	Power 5V	Panel_VCC	
	2	Power 5V	Panel_VCC	
	3	Power 5V	Panel_VCC	
	4	GND	GND	
	5	GND	GND	
	6	GND	GND	
	7	BLVDS data 0 signal-	BLVDS_DN0	
	8	BLVDS data 0 signal+	BLVDS_DP0	
	9	BLVDS data 1 signal-	BLVDS_DN1	
	10	BLVDS data 1 signal+	BLVDS_DP1	
	11	BLVDS data 2 signal-	BLVDS_DN2	
	12	BLVDS data 2 signal+	BLVDS_DP2	
	13	GND	GND	
	14	GND	GND	
	15	BLVDS clock signal-	BLVDS_CKN	
	16	BLVDS clock signal+	BLVDS_CKP	
	17	BLVDS data 3 signal-	BLVDS_DN3	
	18	BLVDS data 3 signal+	BLVDS_DP3	
	19	ALVDS data 0 signal-	ALVDS_DN0	
	20	ALVDS data 0 signal+	ALVDS_DP0	
	21	ALVDS data 1 signal-	ALVDS_DN1	
	22	ALVDS data 1 signal+	ALVDS_DP1	

	23	ALVDS data 2 signal-	ALVDS_DN2	
	24	ALVDS data 2 signal+	ALVDS_DP2	
	25	GND	GND	
	26	GND	GND	
	27	ALVDS clock signal-	ALVDS_CKN	
	28	ALVDS clock signal+	ALVDS_CKP	
	29	ALVDS data 3 signal-	ALVDS_DN3	
	30	ALVDS data 3 signal+	ALVDS_DP3	

Table 4-15 dual LVDS ports Description

Ref	Pin	Function	Name	Comments
J5	1	GND	GND	
	2	GND	GND	
	3	LVDS1 backlight control signal	PWM5	
	4	LVDS1 backlight enabling signal	PH8	
	5	Power 12V	VDD_12V	
	6	Power 12V	VDD_12V	

Table 4-16 LVDS1 backlight Ports

4.11. AUDIO

T507-H series processor also supports one audio output, single end linear output audio signal, audio amplifier chip CS8121SM, the output audio signal is amplified, left and right audio channel output signal through J17 row.

The core board leads the I2S2 signal and the audio coding chip SGTL5000XNAA3 circuit for communication, and develops a 3.5mm headphone interface to output J16.

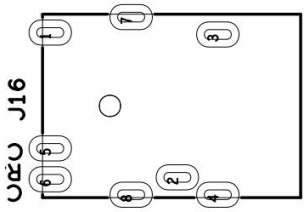

Figure 4-16 Audio Headphoe interface

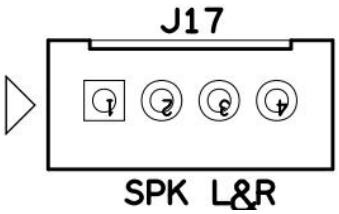

Figure 4 - 17 Audio Amplify interface

4.11.1. Pin Description

Ref	Pin	Function	Name	Comments
J16	1	Audio left channel data output	AUDIO1_LOUT_L	
	2	Audio right channel data output	AUDIO1_LOUT_R	
	3	AUDIO GND	AUDIO_GND	
	4	Audio data entry	AUD_MIC	
	5	NC	NC	
	6	NC	NC	
	7	NC	NC	
	8	NC	NC	

Table 4 - 17 Audio Headphone Interface

Ref	Pin	Function	Name	Comments
J17	1	Left channel output audio+	VO+	
	2	Left channel output audio-	VO-	
	3	Right channel output audio+	VO+	
	4	Right channel output audio-	VO-	

Table 4 - 18 Audio Amplify Interface

4.12. RTC

The RTC standby interface circuit is designed by the evaluation board, and the real-time clock module RX-8025 with I2C bus is used to work with 3.0V external voltage for J27. When the system is powered off, it can be used to maintain the RTC.

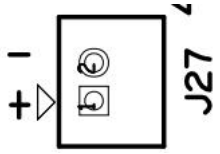

Figure 4-18 RTC battery Ports

4.12.1. Pin Description

Ref	Pin	Function	Name	Comments
J20	1	GND	GND	
	2	Power 3.3V	VDD_BAT	

Table 4-19 RTC battery Interface

4.13. HDMI

The evaluation board is designed with a standard HDMI 2.0A interface that supports 4K @60 FPS playback.

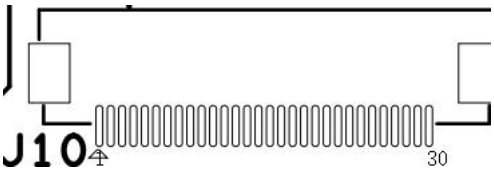

Figure 4-19 HDMI ports

4.13.1. Pin Description

Ref	Pin	Function	Name	Comments
J10	1	HDMI TX2 signal+	TX2R_DP	
	2	GND	GND	
	3	HDMI TX2 signal-	TX2R_DN	
	4	HDMI TX1 signal+	TX1R_DP	
	5	GND	GND	
	6	HDMI TX1 signal-	TX1R_DN	
	7	HDMI TX0 signal+	TX0R_DP	
	8	GND	GND	
	9	HDMI TX0 signal-	TX0R_DN	
	10	HDMI clock signal+	TXR_CKP	
	11	GND	GND	
	12	HDMI clock signal-	TXR_CKN	
	13	HDMI Control signal	HDMI_CEC	
	14	NC	NC	
	15	HDMI I2C clock	HDMI-SCL	
	16	HDMI I2C data	HDMI-SDA	
	17	GND	GND	
	18	HDMI 5V power	VDD5V_HDMI	
	19	EARC Signal detection	HDMI_HPD	
	20	Metal GND	GND_EARTH	
	21	Metal GND	GND_EARTH	
	22	Metal GND	GND_EARTH	
	23	Metal GND	GND_EARTH	

Table 4 - 20 HDMI Interface specification

5. Module description

5.1. 4G LTE

One LTE module interface is reserved for the evaluation board, which can support general Mini P CI-E LTE modules.

MYB-YT507H development board provides Linux driver support and code samples based on Sha nghai Mobile Communication EC20 LTE module. The Mini PCIE connector is from LOTES, the model is AAA PCI-047 PCI-E , the modules and boards are fixed with screw,with good earthquak e resistance. The default power supply voltage of the module is 3.6V, and the control signal is US B2.0 signal, provided by the USB HUB chip.

The carrier board provides one SIM card slot for the 4G module.

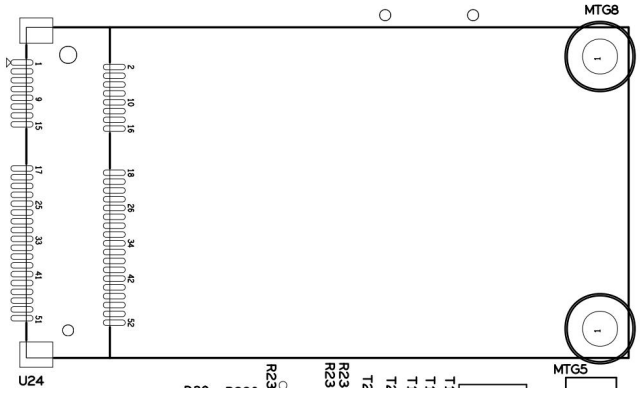

Figure 5-1 4G LTE module Ports

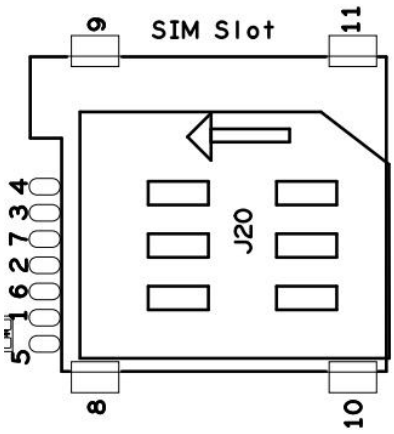

Figure 5-2 SIM Card interface diagram

5.1.1. Pin Description

Ref	Pin	Function	Name	Comments
	36	USB2 HOST data-	USB2-DN	
	38	USB2 HOST data+	USB2-DP	
	22	4G Module reset	4G_RSTIN	
	42	LTE Module indicator	LED	

U24	8	SIM Card Power	USIM_PWR	
	10	SIM Card data	USIM_DATA	
	14	SIM Card Reset	USIM_RESET	
	12	SIM Card clock	USIM_CLK	
	19	4G Module reset	WAKE_IN	
	33	4G Module Power 3.6V	4G_RSTIN	
	24	4G Module Power 3.6V	VDD_LTE	
	2	4G Module Power 3.6V	VDD_LTE	
	39	4G Module Power 3.6V	VDD_LTE	
	41	4G Module Power 3.6V	VDD_LTE	
	52	GND	VDD_LTE	
	4	GND	GND	
	18	GND	GND	
	26	GND	GND	
	40	GND	GND	
	34	GND	GND	
	9	GND	GND	
	15	GND	GND	
	21	GND	GND	
	27	GND	GND	
	29	GND	GND	
	35	GND	GND	
	37	GND	GND	
	43	GND	GND	
	50	GND	GND	
	32	4G module wakes up output	WAKE_OUT	

Table 5-1 4G LTE module interface specification

位号	标识	功能	信号	说明
J20	1	SIM Card Power	USIM_PWR	
	2	SIM Card Reset	USIM_RESET	
	3	SIM Card clock	USIM_CLK	
	4	NC	NC	
	5	GND	GND	
	6	NC	NC	
	7	SIM Card data	USIM_DATA	
	8	GND	GND	
	9	GND	GND	
	10	GND	GND	
	11	GND	GND	

Table 5- 2 SIM Card pin description

5.2. WIFI/BT

MYB-YT507H evaluation board reserved a 2.54mm spacing of 20 pin pin row, to lead SDIO and UART1 with Bluetooth flow interface, corresponding interface J26. You can choose the MY-WF0 05S WIFI Bluetooth module from Mill Tech. Please visit http://www.myir-tech.com/product/MY-WF005S.htm for details on this module.

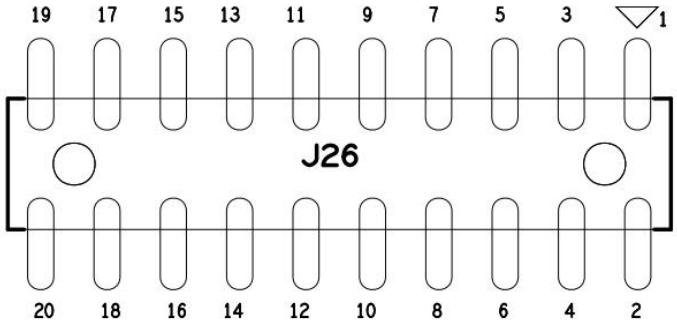

Figure 5-3 WIFI/BT Module Ports

5.2.1. Pin Description

Ref	Pin	Function	Name	Comments
J26	1	NC	NC	
	2	NC	NC	
	3	Power 3.3V	VDD_WIFIBT	
	4	GND	GND	
	5	SDIO data 0	SDIO1-D0	

	6	UART data receive	UART1-RX	
	7	SDIO data 1	SDIO1-D1	
	8	UART data send	UART1-TX	
	9	SDIO data 2	SDIO1-D2	
	10	Bluetooth flow control	UART1-CTS	
	11	SDIO data 3	SDIO1-D3	
	12	Bluetooth flow control	UART1-RTS	
	13	SDIO command signal	SDIO1-CMD	
	14	NC	NC	
	15	GND	GND	
	16	General GPIO	NCSI0-D8	
	17	SDIO clock signal	SDIO1-CLK	
	18	General GPIO	NCSI0-D9	
	19	GND	GND	
	20	General GPIO	NCSI0-D10	

Table 5-3 WIFI/BT ports description

6. Mechanical Size

Core board technology: 43mm*45mm, the board adopts 10 layers of high density PCB design, gol d sinking process production, independent grounding signal layer, lead-free.

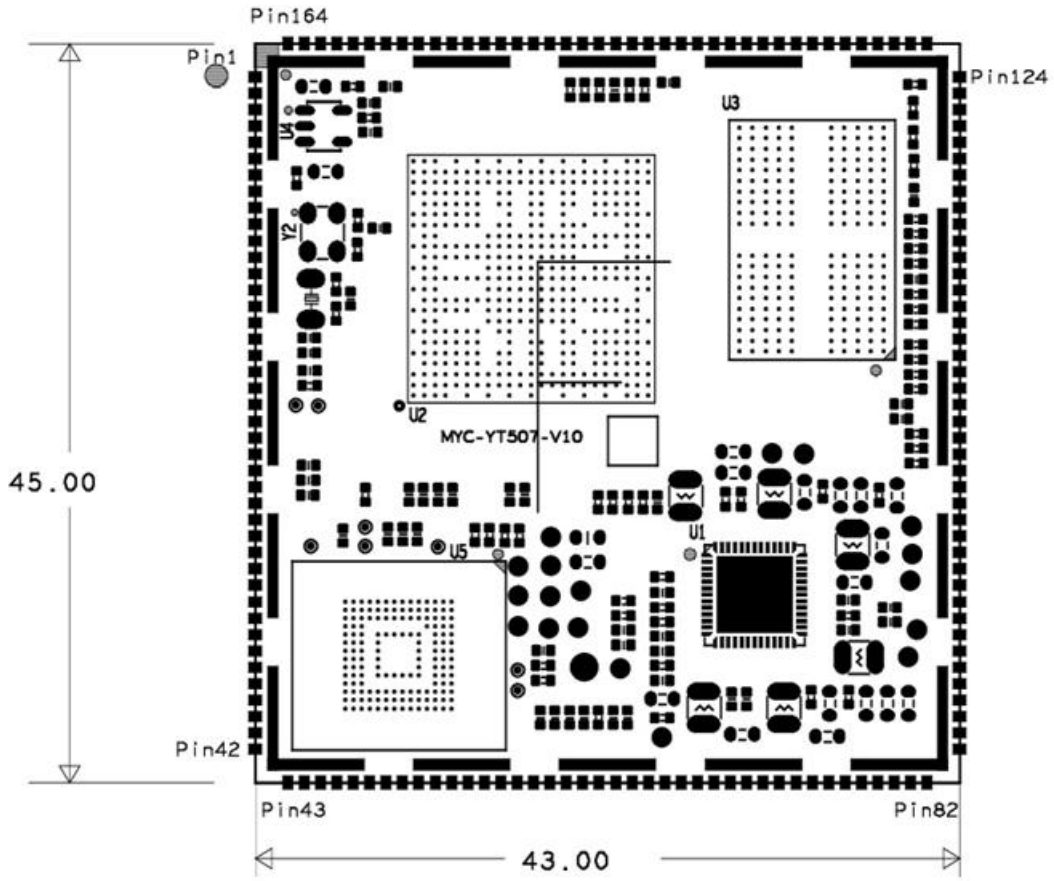

Figure 6 - 1 Core board size

Evaluation plate base plate process: 120 mm x 200mm, 6 layers, gold sink process production, ind ependent grounding signal layer, lead free.

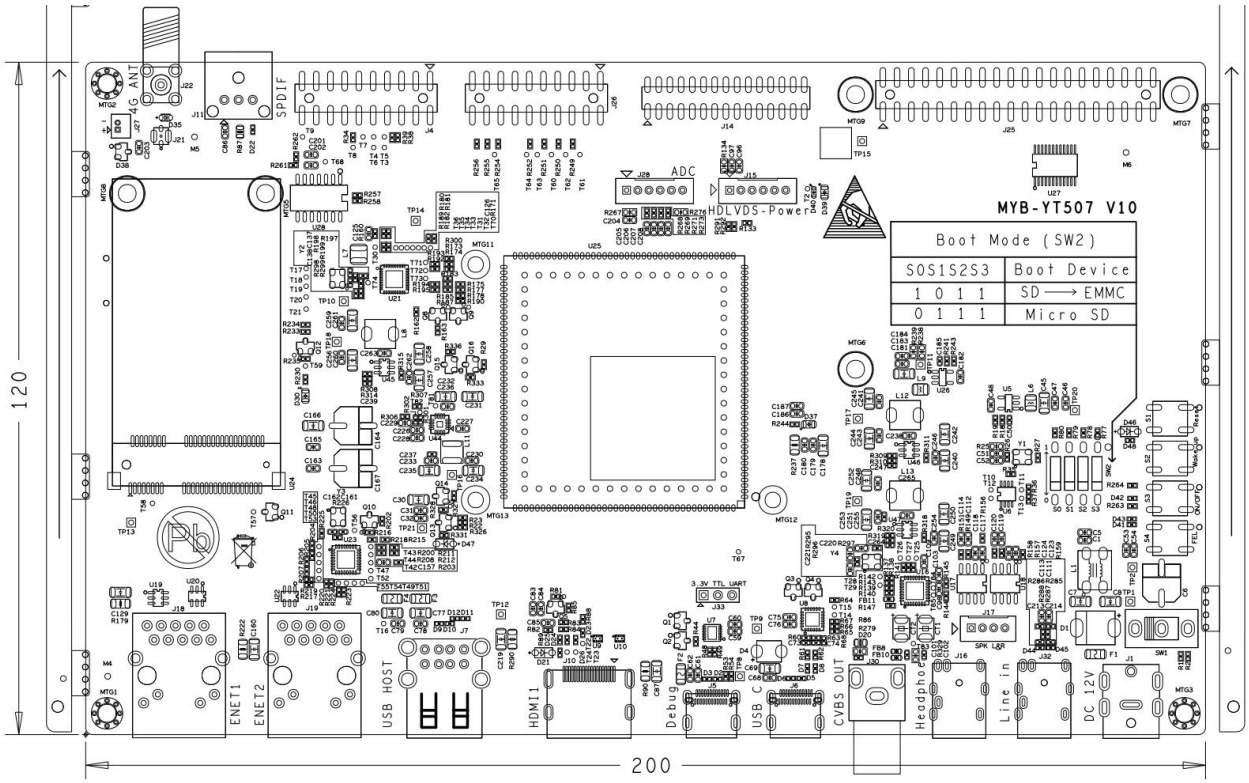

Figure 6 - 2 Evaluation board size

7. EVK Ordering Information

7.1. EVK Part Number

Item	MYD-YT507H-8E1D-150-I	MYD-YT507H-8E1D-150-C
CPU	T507-H	T507-H
Working temperature	-40℃ - +85℃	0℃ - +70℃
DDR	1GB DDR	1GB DDR
EMMC	8GB EMMC	8GB EMMC
WIFI	support	support

Table 7 - 1 Ordering Information 1

Item	MYD-YT507H-8E2D-150-I	MYD-YT507H-8E2D-150-C
CPU	T507-H	T507-H
Working temperature	-40℃ - +85℃	0℃ - +70℃
DDR	2GB DDR	2GB DDR
EMMC	8GB EMMC	8GB EMMC
WIFI	support	support

Table 7 - 2 Ordering Information 2

7.2. Package List

Item	Description
board	X1 EVK board (one core board and one carrier board, both assembled together)
data	x1 quick start guide
wire	X1 Type-c connection cable X1 DC adapter 5.5x2.1 Female to 5.5x1.7 male X1 12V@2A Switching power adapter

Table 7 - 3 Packing List

7.3. Modules supported by EVK

Part Number	Description
MY-CAM003M	5 megapixel MIPI interface camera module
MY-CAM011B	Digital camera module

MY-CAM002U	USB camera (200W pixels)
MY-WF005S	WIFI Bluetooth module
MY-LVDS070C	LVDS interface for 7 "TFTLCD
MY-WiredCom	Raspberry PI interface form, RS232/RS485/CAN

Table 7 - 4 Supported Modules

8. List of Connector

Part Number	Part Name	Manufacture	Ref
Power input	JPD441-N5215-7H	Foxconn	J1
Power switch	SS-12D10-L9-B	XKB	SW1
headset input	JA41131-34BCB-7H	Foxconn	J16
Television Output	AV-8.4-5A	GDZ	J30
Power amplifier output	B4B-PH-K-S	JST	J17
USB C OTG	UT12111-B1609-7F	Foxconn	J6
USB Debug serial port	UT12111-B1609-7F	Foxconn	J5
HDMI	QJ51191-LFB4-7F	Foxconn	J10
USB Host	UB11121-8FDE-4F	Foxconn	J7
100 MBIT Ethernet RJ45	S11-ZZ-0319	UDE	J19
Gigabit Ethernet RJ45	S11-ZZ-0319	UDE	J18
4G module PCIE ports	AAA-PCI-047	Lotes	U24
2-pin RTC battery socket	530470210	Molex	J27
4G module antenna	FC-SMA271	上海飞芯	J22
ADC input	B6B-PH-K-S	JST	J28
Dial the code switch	SSGM640200	ALPS	SW2
Micro SD card slot	WQ21801-B2180-7F	Foxconn	J8
SIM card slot	SI62C-01200	ATOM	J20
DVP camera input	FPC05030-17205	ATOM	J3
LVDS0 displays output	FPC05040-17205	ATOM	J12
LVDS1 displays output	FPC05040-17205	ATOM	J13
MIPI CSI camera input	FPC05024-17205	ATOM	J2

Table 8 - 1 BOM of connectors

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

MYIR Electronics Limited

Room 04, 6th Floor, Building No.2, Fada Road,

Yunli Inteiligent Park, Bantian, Longgang District.

Support Email: support@myirtech.com

Sales Email: sales@myirtech.com

Phone: +86-755-22984836

Fax: +86-755-25532724

Website: www.myirtech.com