MYC-YT507H
Product Manual

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History

Version	Author	Participants	Date	Description
V1.0	Dana		20220413	Initial Version

Contents

1. Overview

Allwinner T5 series is a high-performance quad-core Cortex™-A53 processor, suitable for the new generation of automotive market. T5 series meet the test requirements of automobile AEC - Q100. The chip integrates quad-core Cortex™-A53 CPU, G31 MP2 GPU, 32-bit DDR3 / LPDDR3 / DDR4 / LRDDR4 dynamic random access memory. Multi-channel video output interface (RGB / 2*LVDS / HDMI / CVBS OUT), multi-channel video input interface (MIPI CSI/ BT656/BT1120). The chip supports 4K@60fps H.265 decoding, 4K@60fps VP9 decoding, 4K@60fps AVS2 decoding, 4K@25fps H.264 encoding, 3D noise reduction as well as automatic color matching system and trapezoidal correction module to provide a smooth user experience and professional visual effects.

MYC-YT507H core board is based on T507-H processor, has a good software development environment, kernel support open source operating system Linux. MYC-YT507H also has rich interface resources. You may download the above materials at any time at the following address:

http://d.myirtech.com//MYD-YT507H/

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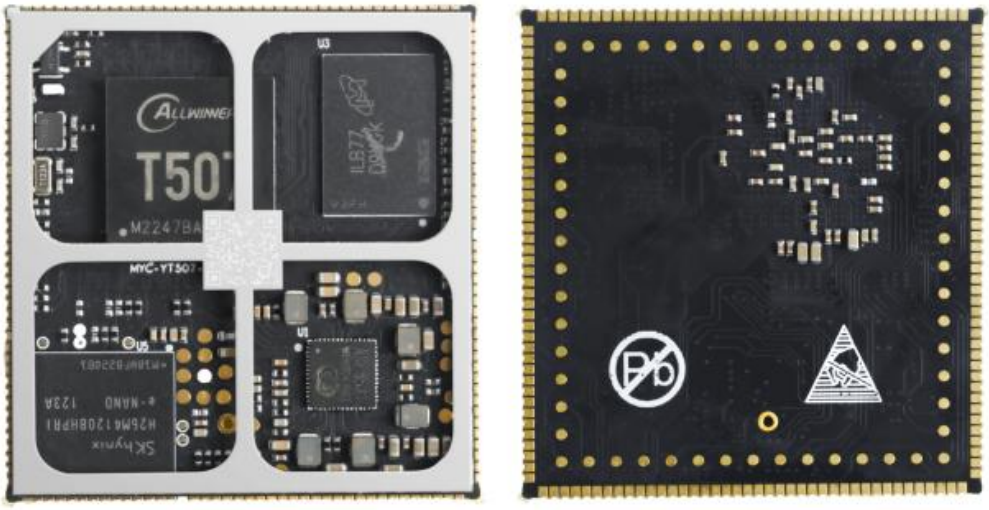

Figure 1-1 MYC-YT507H Core board

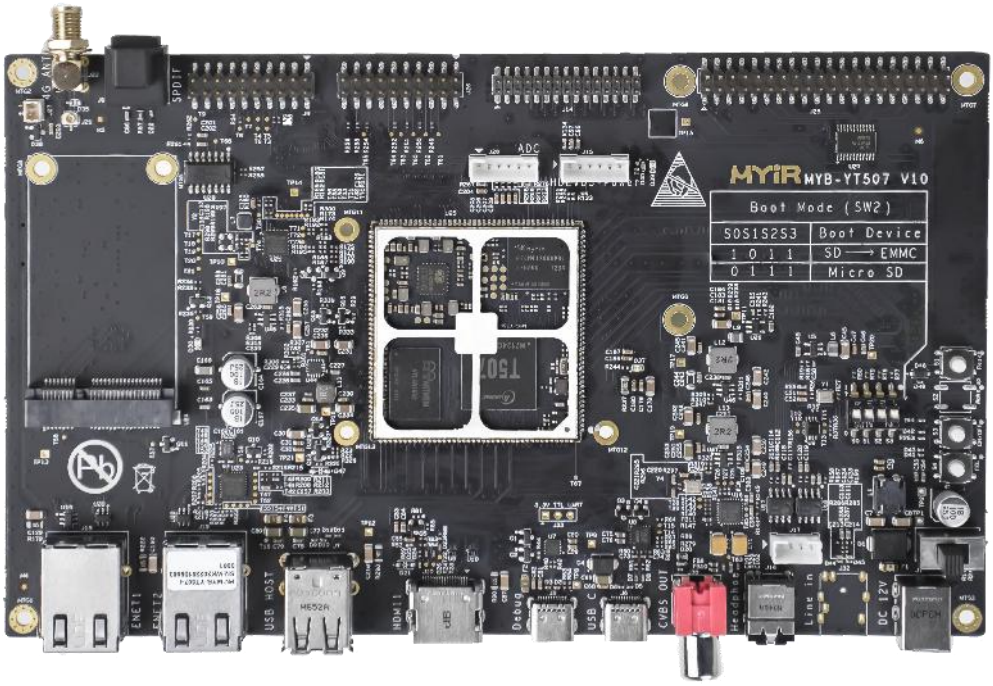

Figure 1-2 MYD-YT507H Kit Top side

Figure 1-3 MYD-YT507H Kit Bottom side

2. Product Presentation

MYC-YT507H core board adopts SMD encapsulation form patch (stamp hole + back pad). There are 4 standard models. They have some differences in storage configuration, temperature and other aspects, customers can choose the appropriate model according to their needs. For the differences between product models, see 2.4.

2.1. Chip Resources

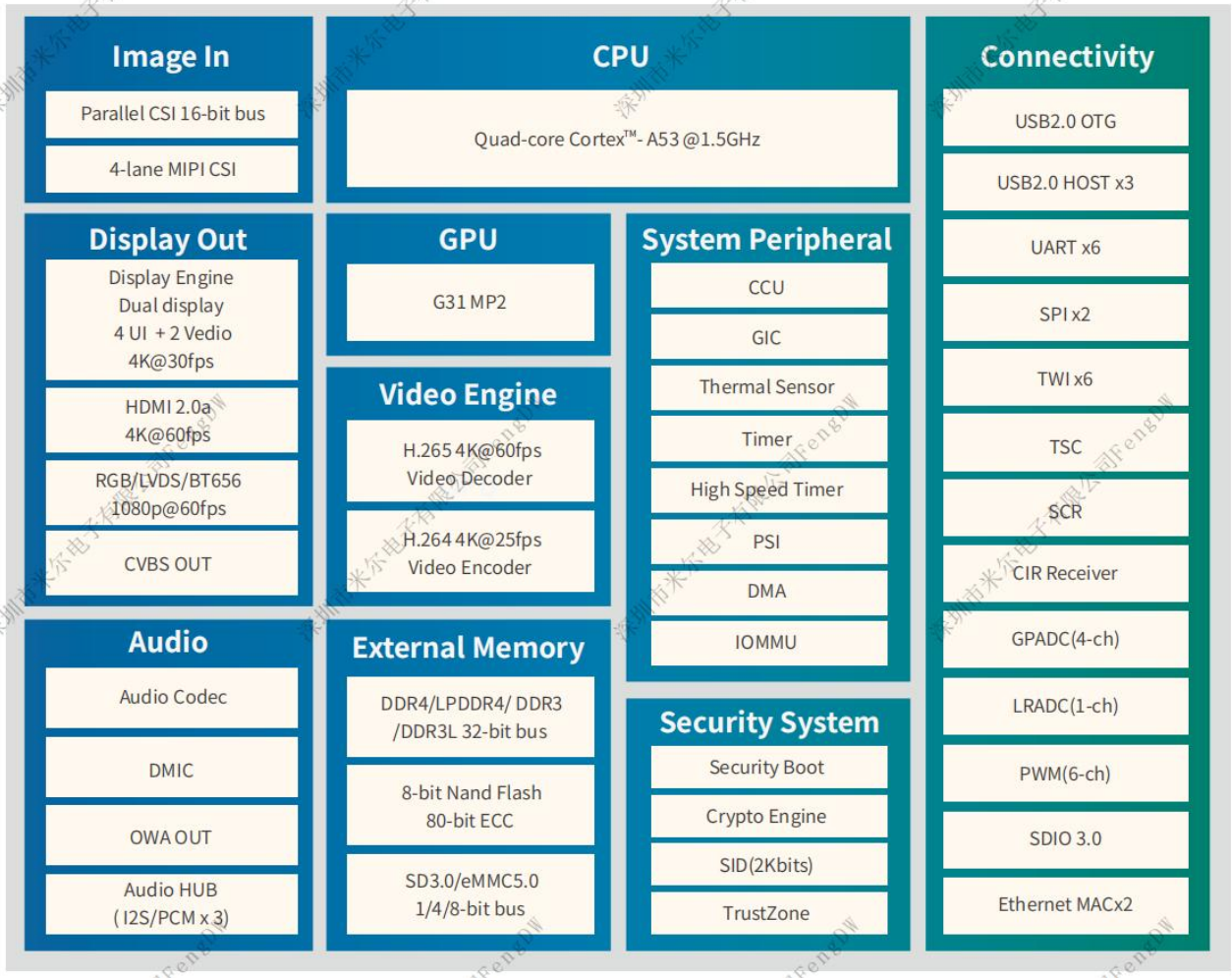

Figure 2-1 T507-H Resource diagram

Resource	Parameter Description
CPU	● Quad-core ARM Cortex™-A53@1.5Ghz
GPU	● G31 MP2 ● Supports OpenGL ES 3.2/2.0/1.0,Vulkan 1.1, OpenCL 2.0
External storage	● 32-bit DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 interface, supporting maximum capacity of 4GB ● SD3.0/eMMC5.0 interface

	● 8-bit Nand flash interface with maximum 80-bit/1KB ECC
Video engine	**Video decoder** ● H.265 MP decoder up to 4K@60fps ● H.264 BL/MP/HP decoder up to 4K@30fps ● VP9 decoder up to 4K@60fps ● AVS2 decoder up to 4K@60fps ● Multi-format 1080p@60fps video playback, including VP8, MPEG1/2 SP/MP,MPEG4 SP/ASP, ● AVS+/AVS JIZHUN, VC1 SP/MP **Video encoder** ● H.264 encoder up to 4K@25fps ● MJPEG encoder up to 4K@15fps ● JPEG encoder up to 8K x 8K resolution
Video input	● Supports one 8-/10-/12-/16-bit digital camera(DC) interface ● Maximum pixel clock of 148.5MHz for each DC interface ● BT656,BT1120 video input for multichannel YUV ● Four-lane MIPI CSI, up to 1 Gbps per lane in HS transmission,compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00 ● Maximum video capture resolution of 8M@30fps or 4x 1080p@25fps for MIPI CSI ● Supports formats:YUV422,YUV420,RAW-8,RAW-10,RAW-12
Audio	● Two DAC channels ● Supports 1 audio output interface (differential LINEOUTP/N or single-end LINEOUTL/LINEOUTR) ● One Audio HUB, supporting internal mixing function ● Embedded 3 I2S/PCM for connecting the external devices (I2S0 for extended audio codec, I2S2 for BT, I2S3 for digital power amplifier) ● Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode ● I2S mode supports 8 channels, and 32-bit/192kbit sample rate ● I2S and TDM-modes support maximum 16 channels, and 32-bit/96kbit sample rate ● One OWA OUT interface, supporting 16-/20-/24-bit outputs ● Integrated digital microphone, supporting maximum 8 digital PDM microphones
Display output	● HDMI 2.0a up to 4K@60fps ● TV CVBS output, supporting PAL/NTSC ● LVDS interface with dual link, up to 1080p@60fps ● RGB interface with DE/SYNC mode, up to 1080p@60fps
Security engine	● Supports Full Disk Encryption ● AES, DES, 3DES, and XTS encryption and decryption algorithms ● MD5, SHA, and HMAC tamper proofing

	● RSA, ECC signature and verification algorithms ● Supports 160-bit hardware pseudo random number generator(PRNG) with 175-bit seed ● Supports 256-bit hardware true random number generator(TRNG) ● Integrated 2K-bit EFUSE for chip ID and security application
connection	● 3 x USB2.0 Host, 1 x USB2.0 OTG ● 2 x Ethernet MAC (one 10/100 Mbps Ethernet port with RMII interface, one 10/100/1000 Mbps ● Ethernet port with RGMII and RMII interfaces) ● SDIO 3.0, TSC, SCR, CIR Receiver ● 6 x TWI, 2 x SPI, 6 x UART ● 6-ch PWM, 4-ch GPADC. 1-ch LRADC
PMIC	● Allwinner Power Management IC
encapsulation	● TFBGA 421balls ● 15 mm x 15 mm size,0.65 mm ball pitch,0.35 mm ball size
Process technology	● 28nm HPC

Table 2-1 T507-H resource

Refer to the chip manual for details.

2.2. Core Board Features

Item	features
CPU series	T5 Series
CPU model	T507-H
Processor CPU	x4 ARM Cortex™-A53
DDR storage	LPDDR4 1GB/2GB
eMMC	EMMC 8GB (Other capacity optional)
Core board size	43 x 45 x 3.5 mm (With shielded skeleton)
interface type	SMD patch，Stamp hole+LGA
PCB board specifications	10-layer board design, gold immersion process
operating system	Linux 4.9

Table 2-2 Core board features

2.3. Block Diagram

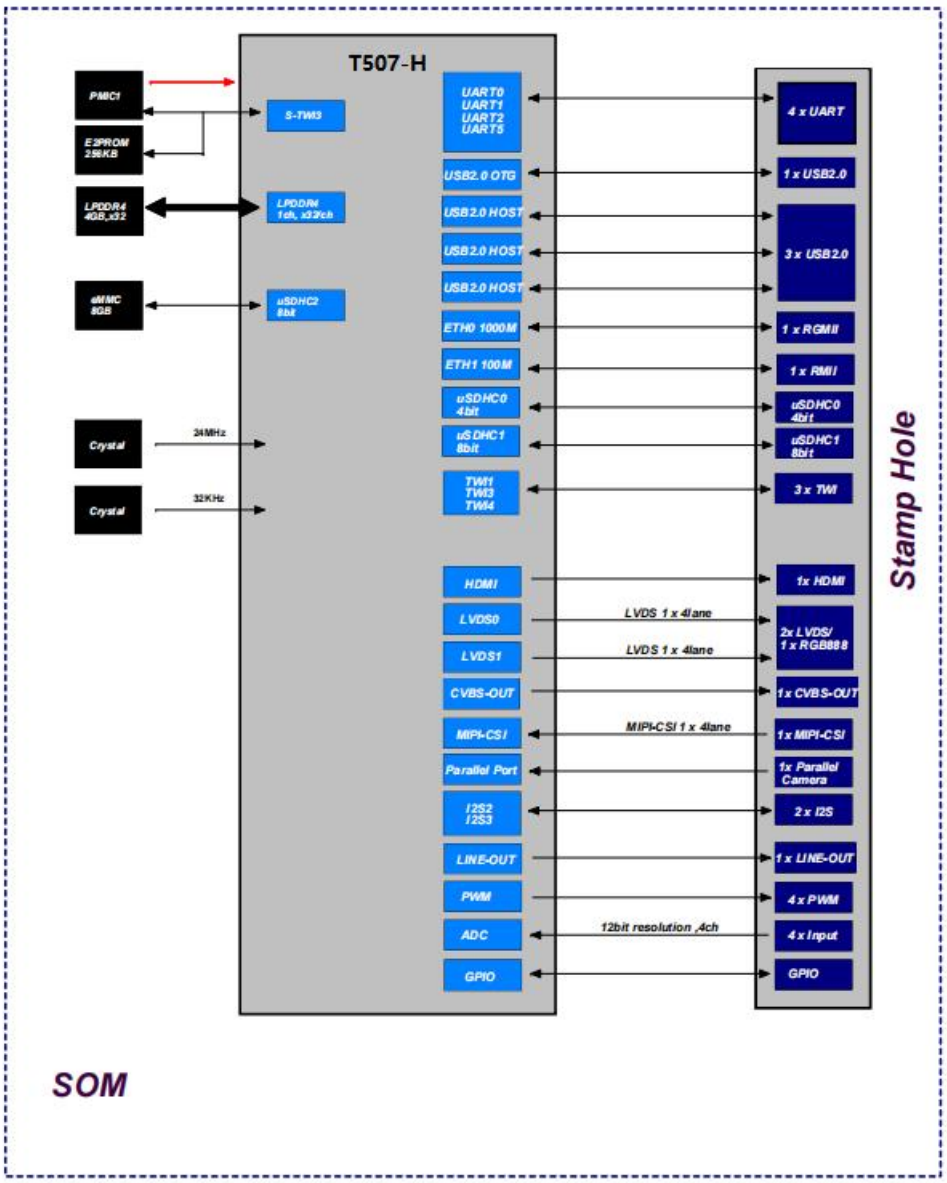

Figure 2-2 Core board block diagram

2.4. Core Board Ordering Information

MYC-YT507H core board have 4 models according to the different parameters of core board storage device and operating temperature. Please select the model most suitable for you from the following list.

Part No. / Item	MYC-YT507H-8E1D-150-I	MYC-YT507H-8E1D-150-C
CPU	T507-H	T507-H
CPU series	T5 Series	T5 Series
Core	x4 Cortex™-A53	x4 Cortex™-A53
Frequency	1.5Ghz	1.5Ghz
System	Linux 4.9	Linux 4.9
DDR	1GB LPDDR4	1GB LPDDR4
eMMC	8GB eMMC	8GB eMMC
Video input	1 DVP camera input 1 MIPI CSI input	1 DVP camera input 1 MIPI CSI input
Display output	1 HDMI 2.0a, support 4K@60fps 1 TV CVBS output, support PAL/NTSC 2 LVDS / 1 HD LVDS / RGB888, up to support 1080p@60fps	1 HDMI 2.0a, support 4K@60fps 1 TV CVBS output, support PAL/NTSC 2 LVDS / 1 HD LVDS / RGB888, up to support 1080p@60fps
Touch screen	Support Capacitive touch Support 4-wire resistive screen (touch chip is required)	Support Capacitive touch Support 4-wire resistive screen (touch chip is required)
UART	6 way (Max)	6 way (Max)
CAN	NO	NO
USB2.0	3 USB Host +1 USB OTG	3 USB Host +1 USB OTG
Ethernet	1 RGMII +1 RMII	1 RGMII +1 RMII
I2C	6 (Max)	6 (Max)
SPI	2 (Max)	2 (Max)
GPIO	138	138
ADC	5	5
Power Supply	+5V	+5V
Mechanical size	43 x 45 x 3.5 mm	43 x 45 x 3.5 mm
Operating temperature	-40℃ - +85℃	0℃ - +70℃
Connector	Stamp hole+LGA (222 PIN)	Stamp hole+LGA (222 PIN)
Certification	CE ROHS	CE ROHS

Table 2-3 MYC-YT507H core board ordering information 1

Part No. / Item	MYC-YT507H-8E2D-150-I	MYC-YT507H-8E2D-150-C
CPU	T507-H	T507-H
CPU series	T5 Series	T5 Series
Core	x4 Cortex™-A53	x4 Cortex™-A53
Frequency	1.5Ghz	1.5Ghz
System	Linux 4.9	Linux 4.9
DDR	2GB LPDDR4	2GB LPDDR4
eMMC	8GB eMMC	8GB eMMC
Video input	1 DVP camera input 1 MIPI CSI input	1 DVP camera input 1 MIPI CSI input
Display output	1 HDMI 2.0a, support 4K@60fps 1 TV CVBS output, support PAL/NTSC 2 LVDS / 1 HD LVDS / RGB888, up to support 1080p@60fps	1 HDMI 2.0a, support 4K@60fps 1 TV CVBS output, support PAL/NTSC 2 LVDS / 1 HD LVDS / RGB888, up to support 1080p@60fps
Touch screen	Support Capacitive touch Support 4-wire resistive screen (touch chip is required)	Support Capacitive touch Support 4-wire resistive screen (touch chip is required)
UART	6 way (Max)	6 way (Max)
CAN	NO	NO
USB2.0	3 USB Host +1 USB OTG	3 USB Host +1 USB OTG
Ethernet	1 RGMII +1 RMII	1 RGMII +1 RMII
I2C	6 (Max)	6 (Max)
SPI	2 (Max)	2 (Max)
GPIO	138	138
ADC	5	5
Power Supply	+5V	+5V
Mechanical size	43 x 45 x 3.5 mm	43 x 45 x 3.5 mm
Operating temperature	-40℃ - +85℃	0℃ - +70℃
Connector	Stamp hole+LGA (222 PIN)	Stamp hole+LGA (222 PIN)
Certification	CE ROHS	CE ROHS

Table 2-4 MYC-YT507H core board ordering information 2

3. Pin Description

3.1. Pin Out

MYC-YT507H core board is welded to the carrier board in the form of SMD patch, and the pin contains a stamp hole and a back pad. For bottom plate packaging design, refer to the instructions in Section 7.2.

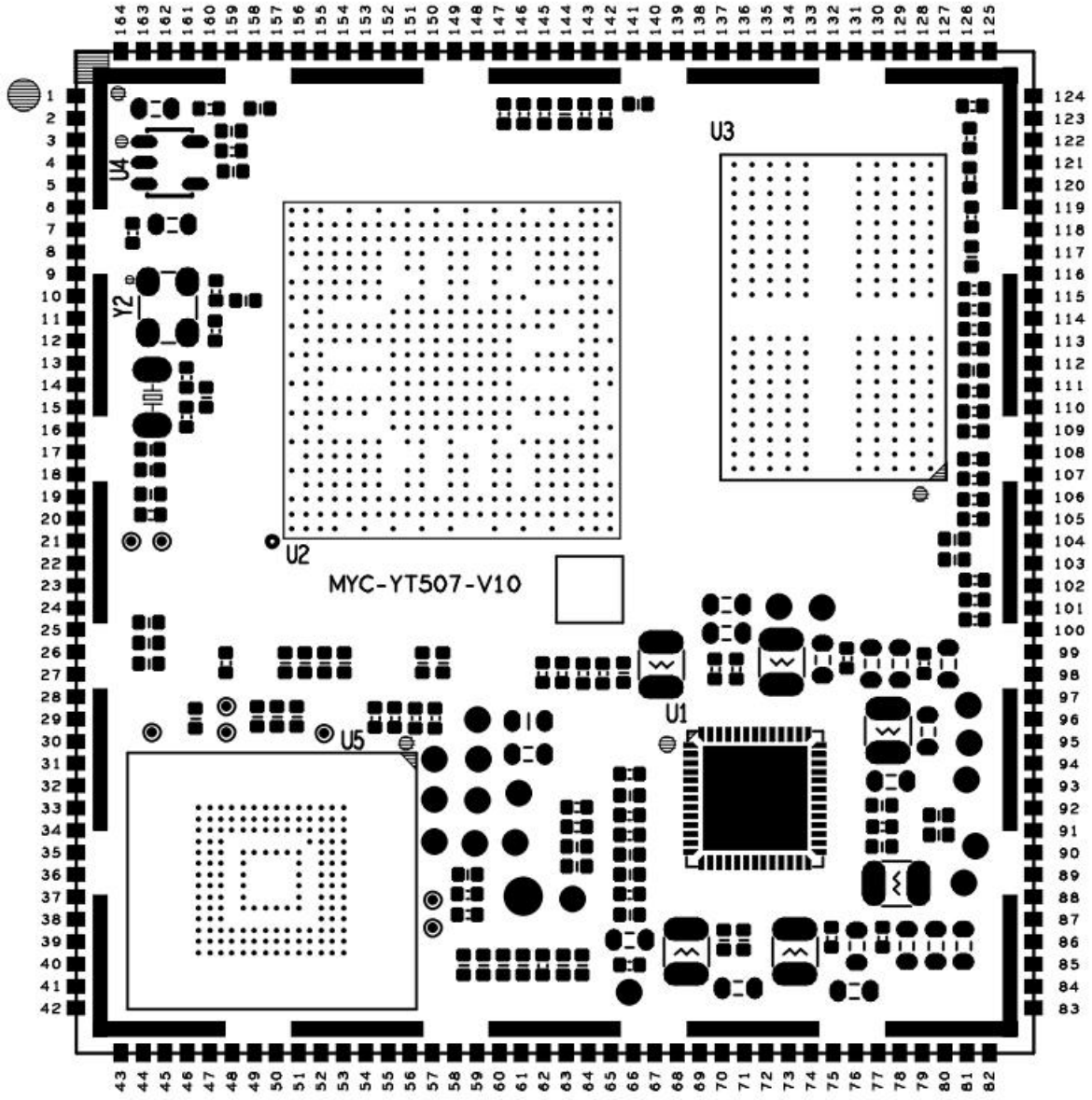

Figure 3-1 Module pin at top side

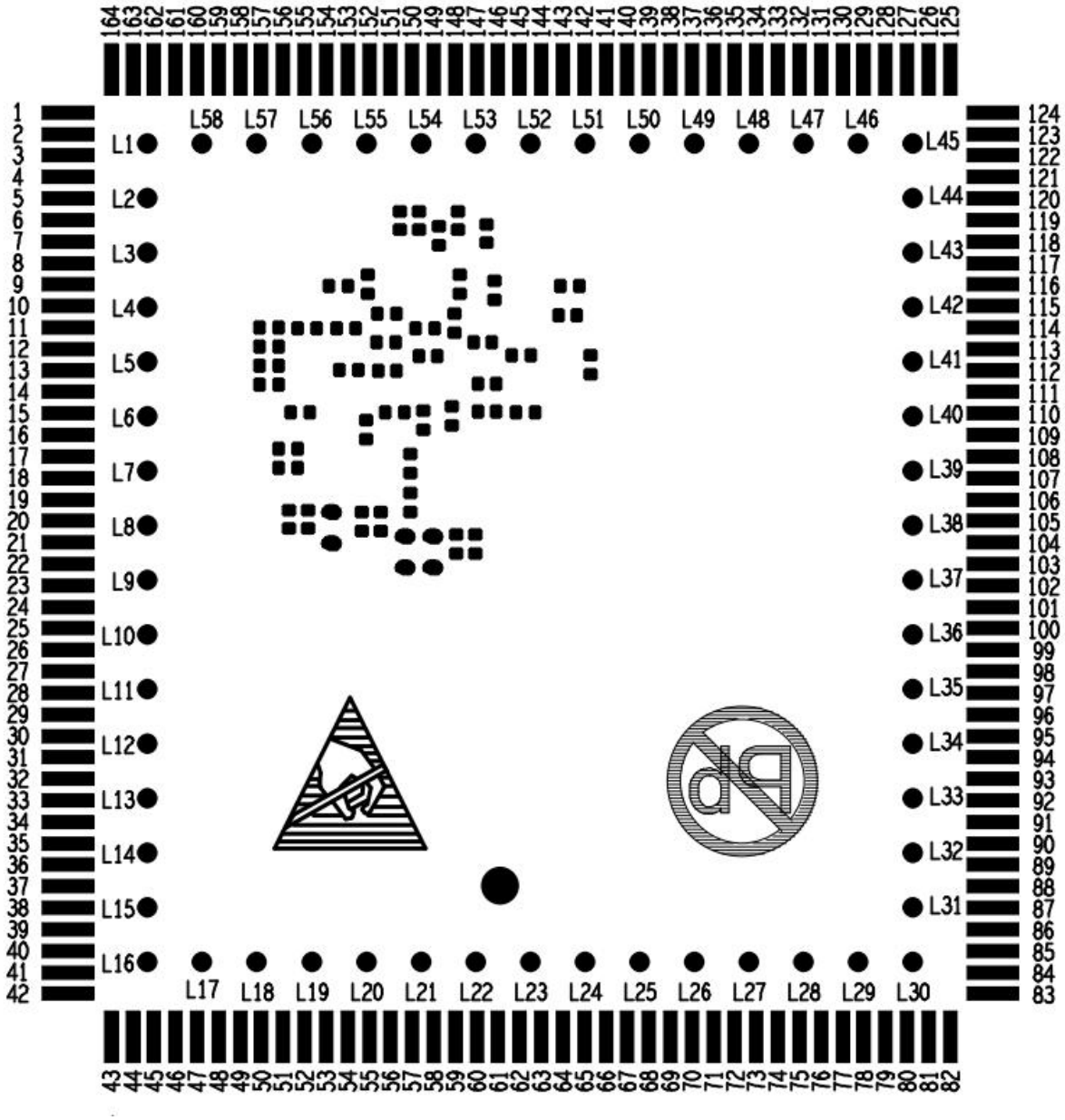

Figure 3-2 Module pin at bottom side

3.2. Pin List

The definition of MYC-YT507H core board interface pins is shown in the following table. The pin functions of BSP development package are configured according to "Default functions" in the following table. If you need to change the default pin functions, please modify the relevant driver configuration code; otherwise, uncertain exceptions such as driver conflict may occur.

Pin	Signal	Default Function	Description	Voltage	IO	Comments
1	VSOM-5V	VSOM-5V	5.0 V power supply	5V	I	
2	VSOM-5V	VSOM-5V	5.0 V power supply	5V	I	
3	VSOM-5V	VSOM-5V	5.0 V power supply	5V	I	
4	VSOM-5V	VSOM-5V	5.0 V power supply	5V	I	
5	VSOM-3V3	VSOM-3V3	3.3V output	3.3V	O	
6	VSOM-3V3	VSOM-3V3	3.3V output	3.3V	O	
7	VCC-USB2-3V3	VCC-USB2-3V3	USB2 supports standby wake-up	3.3V	O	Design base plate this pin is reserved not to use
8	GND	GND	GND	0V		
9	CPU-RESET	CPU-RESET	Low level causes reset	1.8V	I	Design base plate this pin is reserved not to use
10	CPU-ONOFF	CPU-ONOFF	External button	1.8V	I	
11	PMIC-WAKEUP	NC	NC	—	—	Design base plate this pin is reserved not to use
12	GND	GND	GND	0V	—	
13	LVDS1-D1N	LVDS1-D1N	LVDS1 differential data 1-	3.3V	O	RGB multiplexing interface
14	LVDS1-D1P	LVDS1-D1P	LVDS1 differential data 1+	3.3V	O	RGB multiplexing interface
15	GND	GND	GND			
16	LVDS1-D3N	LVDS1-D3N	LVDS1 differential data 3-	3.3V	O	RGB multiplexing interface
17	LVDS1-D3P	LVDS1-D3P	LVDS1 differential data 3+	3.3V	O	RGB multiplexing interface
18	GND	GND	GND	0V	—	
19	LVDS1-D2N	LVDS1-D2N	LVDS1 differential data 2-	3.3V	O	RGB multiplexing interface
20	LVDS1-D2P	LVDS1-D2P	LVDS1 differential data 2+	3.3V	O	RGB multiplexing interface
21	GND	GND	GND	0V	—	
22	LVDS1-CLKN	LVDS1-CLKN	LVDS1 differential clock -	3.3V	O	RGB multiplexing interface
23	LVDS1-CLKP	LVDS1-CLKP	LVDS1 differential clock +	3.3V	O	RGB multiplexing interface
24	GND	GND	GND	0V	—	
25	LVDS1-D0N	LVDS1-D0N	LVDS1 differential data 1-	3.3V	O	RGB multiplexing interface
26	LVDS1-D0P	LVDS1-D0P	LVDS1 differential data 1+	3.3V	O	RGB multiplexing interface
27	GND	GND	GND	0V	—	
28	LVDS0-D2N	LVDS0-D2N	LVDS0 differential data 2-	3.3V	O	RGB multiplexing interface
29	LVDS0-D2P	LVDS0-D2P	LVDS0 differential data 2+	3.3V	O	RGB multiplexing interface
30	GND	GND	GND	0V	—	
31	LVDS0-D1N	LVDS0-D1N	LVDS0 differential data 1-	3.3V	O	RGB multiplexing interface
32	LVDS0-D1P	LVDS0-D1P	LVDS0 differential data 1+	3.3V	O	RGB multiplexing interface
33	GND	GND	GND	0V	—	
34	LVDS0-D0N	LVDS0-D0N	LVDS0 differential data 0-	3.3V	O	RGB multiplexing interface
35	LVDS0-D0P	LVDS0-D0P	LVDS0 differential data 0+	3.3V	O	RGB multiplexing interface
36	GND	GND	GND	0V	—	

37	LVDS0-CLKN	LVDS0-CLKN	LVDS0 differential clock -	3.3V	O	RGB multiplexing interface
38	LVDS0-CLKP	LVDS0-CLKP	LVDS0 differential clock +	3.3V	O	RGB multiplexing interface
39	GND	GND	GND	0V	—	
40	LVDS0-D3N	LVDS0-D3N	LVDS0 differential data 3-	3.3V	O	RGB multiplexing interface
41	LVDS0-D3P	LVDS0-D3P	LVDS0 differential data 3+	3.3V	O	RGB multiplexing interface
42	GND	GND	GND	0V	—	
43	NCSI0-SCK	NCSI0-SCK	Parallel CSI I2C clock	3.3V	O	
44	NCSI0-SDA	NCSI0-SDA	Parallel CSI I2C data	3.3V	I/O	
45	NCSI0-HSYNC	NCSI0-HSYNC	Parallel CSI Line sync signal	3.3V	I	
46	NCSI0-D7	NCSI0-D7	Parallel CSI data 7	3.3V	I	
47	NCSI0-PCLK	NCSI0-PCLK	Parallel CSI input pixel clock	3.3V	I	
48	NCSI0-D6	NCSI0-D6	Parallel CSI data 6	3.3V	I	
49	NCSI0-D5	NCSI0-D5	Parallel CSI data 5	3.3V	I	
50	NCSI0-D3	NCSI0-D3	Parallel CSI data 3	3.3V	I	
51	NCSI0-D2	NCSI0-D2	Parallel CSI data 2	3.3V	I	
52	NCSI0-D4	NCSI0-D4	Parallel CSI data 4	3.3V	I	
53	NCSI0-D0	NCSI0-D0	Parallel CSI data 0	3.3V	I	
54	NCSI0-D1	NCSI0-D1	Parallel CSI data 1	3.3V	I	
55	NCSI0-VSYNC	NCSI0-VSYNC	Parallel CSI field sync signal	3.3V	I	
56	NCSI0-D15	NCSI0-D15	Parallel CSI data 15	3.3V	I	
57	CSI-FSIN0	CSI-FSIN0	Reserved unused	3.3V	I	
58	NCSI0-D14	NCSI0-D14	Parallel CSI data 14	3.3V	I	
59	NCSI0-D13	NCSI0-D13	Parallel CSI data 13	3.3V	I	
60	NCSI0-MCLK	NCSI0-MCLK	Parallel CSI output clock	3.3V	O	
61	NCSI0-D12	NCSI0-D12	Parallel CSI data 12	3.3V	I	
62	NCSI0-D11	NCSI0-D11	Parallel CSI data 11	3.3V	I	
63	NCSI0-D10	NCSI0-D10	Parallel CSI data 10	3.3V	I	
64	NCSI0-D9	NCSI0-D9	Parallel CSI data 9	3.3V	I	
65	NCSI0-D8	NCSI0-D8	Parallel CSI data 8	3.3V	I	
66	GND	GND	GND	0V	—	
67	RGMII-MDC	RGMII-MDC	RGMII Manage Data Clock	3.3V	O	
68	RGMII-RXD1	RGMII-RXD1	RGMII data receive 1	3.3V	I	
69	GPHY_RST	GPHY_RST	PHY chip reset	3.3V	O	
70	RGMII-RXCTL	RGMII-RXCTL	RGMII data receive effective	3.3V	I	
71	RGMII-RXD2	RGMII-RXD2	RGMII data receive 2	3.3V	I	
72	RGMII-RXD0	RGMII-RXD0	RGMII data receive 0	3.3V	I	
73	GND	GND	GND	0V	—	
74	RGMII-CLKIN-125M	RGMII-CLKIN-125M	RGMII MAC Parameter clock	3.3V	I	
75	GND	GND	GND	0V	—	
76	RGMII-RXD3	RGMII-RXD3	RGMII data receive 3	3.3V	I	
77	RGMII-RXCK	RGMII-RXCK	RGMII Receive clock	3.3V	I	
78	RGMII-MDIO	RGMII-MDIO	RGMII Manage Data	3.3V	I/O	
79	GPHY-CLK-25M	GPHY-CLK-25M	25Mhz Clock output	3.3V	O	
80	RGMII-TXD1	RGMII-TXD1	RGMII Data sent 1	3.3V	O	
81	RGMII-TXD3	RGMII-TXD3	RGMII Data sent 3	3.3V	O	

82	RGMII-TXCTL	RGMII-TXCTL	RGMII Send control	3.3V	O	
83	NC	NC	NC			
84	GND	GND	GND	0V	—	
85	RGMII-TXCK	RGMII-TXCK	RGMII Send clock	3.3V	O	
86	GND	GND	GND	0V	—	
87	RGMII-TXD0	RGMII-TXD0	RGMII Data sent 0	3.3V	O	
88	RGMII-TXD2	RGMII-TXD2	RGMII Data sent 2	3.3V	O	
89	GND	GND	GND	0V	—	
90	SDIO0-D2	SDIO0-D2	SDIO0 Data 2	3.3V	I/O	
91	SDIO0-CMD	SDIO0-CMD	SDIO0 command	3.3V	O	
92	SDIO0-D1	SDIO0-D1	SDIO0 Data 1	3.3V	I/O	
93	SDIO0-CLK	SDIO0-CLK	SDIO0 clock	3.3V	O	
94	SDIO1-D3	SDIO1-D3	SDIO1 Data 3	3.3V	I/O	
95	SDIO1-D1	SDIO1-D1	SDIO1 Data 1	3.3V	I/O	
96	SDIO0-D3	SDIO0-D3	SDIO0 Data 3	3.3V	I/O	
97	SDIO0-D0	SDIO0-D0	SDIO0 Data 0	3.3V	I/O	
98	SDIO1-CLK	SDIO1-CLK	SDIO1 clock	3.3V	O	
99	SDIO1-D2	SDIO1-D2	SDIO1 Data 2	3.3V	I/O	
100	SDIO1-CMD	SDIO1-CMD	SDIO1 command	3.3V	O	
101	SDIO1-D0	SDIO1-D0	SDIO1 Data 0	3.3V	I/O	
102	SDIO0-DET	SDIO0-DET	SDIO0 Card Plug detection	3.3V	I	
103	GND	GND	GND	0V	—	
104	MCSI-MCLK	MCSI-MCLK	MIPI CSI Base clock output	-	I	
105	MCSI-SDA	MCSI-SDA	MIPI CSI I2C Data	-	I	
106	MCSI-SCK	MCSI-SCK	MIPI CSI I2C clock	-	I	
107	GND	GND	GND	0V	—	
108	MCSI-CLKP	MCSI-CLKP	MIPI CSI differential clock+	-	I	
109	MCSI-CLKN	MCSI-CLKN	MIPI CSI differential clock-	-	I	
110	GND	GND	GND	0V	—	
111	MCSI-D0P	MCSI-D0P	MIPI CSI differential data 0+	-	I	
112	MCSI-D0N	MCSI-D0N	MIPI CSI differential data 0-	-	I	
113	GND	GND	GND	0V	—	
114	MCSI-D1P	MCSI-D1P	MIPI CSI differential data 1+	-	I	
115	MCSI-D1N	MCSI-D1N	MIPI CSI differential data 1-	-	I	
116	GND	GND	GND	0V	—	
117	MCSI-D2P	MCSI-D2P	MIPI CSI differential data 2+	-	I	
118	MCSI-D2N	MCSI-D2N	MIPI CSI differential data 2-	-	I	
119	GND	GND	GND	0V	—	
120	MCSI-D3P	MCSI-D3P	MIPI CSI differential data 3+	-	I	
121	MCSI-D3N	MCSI-D3N	MIPI CSI differential data 3-	-	I	
122	GND	GND	GND	0V	—	
123	TV-OUT	TV-OUT	Analog video output	0~1.8V	O	
124	GND	GND	GND	0V	—	
125	HDMI-CEC	HDMI-CEC	HDMI CEC signal	1.8V	I	
126	HDMI-SDA	HDMI-SDA	HDMI Serial data	1.8V	I/O	
127	HDMI-SCL	HDMI-SCL	HDMI serial clock	1.8V	O	

128	HDMI-HPD	HDMI-HPD	HDMI Hot swap signal	1.8V	I	
129	GND	GND	GND	0V	—	
130	HTXCP	HTXCP	HDMI TMDS Differential clock signal+	-	O	
131	HTXCN	HTXCN	HDMI TMDS Differential clock signal-	-	O	
132	GND	GND	GND	0V	—	
133	HTX1P	HTX1P	HDMI TMDS Differential data 1+	-	O	
134	HTX1N	HTX1N	HDMI TMDS Differential data 1-	-	O	
135	GND	GND	GND	0V	—	
136	HTX0P	HTX0P	HDMI TMDS Differential data 0+	-	O	
137	HTX0N	HTX0N	HDMI TMDS Differential data 0-	-	O	
138	GND	GND	GND	0V	—	
139	HTX2P	HTX2P	HDMI TMDS Differential data 2+	-	O	
140	HTX2N	HTX2N	HDMI TMDS Differential data 2-	-	O	
141	GND	GND	GND	0V	—	
142	USB0-DN	USB0-DN	USB0 Differential signal-	-	I/O	
143	USB0-DP	USB0-DP	USB0 Differential signal+	-	I/O	
144	GND	GND	GND	0V	—	
145	USB1-DN	USB1-DN	USB1 Differential signal-	-	I/O	
146	USB1-DP	USB1-DP	USB1 Differential signal+	-	I/O	
147	GND	GND	GND	0V	—	
148	USB2-DN	USB2-DN	USB2 Differential signal-	-	I/O	
149	USB2-DP	USB2-DP	USB2 Differential signal+	-	I/O	
150	GND	GND	GND	0V	—	
151	USB3-DN	USB3-DN	USB3 Differential signal-	-	I/O	
152	USB3-DP	USB3-DP	USB3 Differential signal+	-	I/O	
153	GND	GND	GND	0V	—	
154	RMII-TXEN	RMII-TXEN	RMII send enable	3.3V	O	
155	RMII-TXCK	RMII-TXCK	RMII send clock	3.3V	O	
156	RMII-RXD1	RMII-RXD1	RMII Data receive 1	3.3V	I	
157	RMII-CRS-RXDV	RMII-CRS-RXDV	RMII Carrier sense data received effective	3.3V	I	
158	RMII-RXD0	RMII-RXD0	RMII Data receive 0	3.3V	I	
159	RMII-RXER	RMII-RXER	RMII Receive error	3.3V	I	
160	RMII-MDIO	RMII-MDIO	RMII Manage data	3.3V	I/O	
161	RMII-MDC	RMII-MDC	RMII Manage clock	3.3V	O	
162	RMII-TXD0	RMII-TXD0	RMII data send 0	3.3V	O	
163	RMII-TXD1	RMII-TXD1	RMII data send 1	3.3V	O	
164	EPHY_RST	EPHY_RST	PHY chip reset	3.3V	O	
L1	UART5-TX	UART5-TX	UART5 data send	3.3V	O	

L2	UART5-RX	UART5-RX	UART5 data receive	3.3V	I	
L3	UART0-TX	UART0-TX	Debug UART0 data send	3.3V	O	
L4	UART0-RX	UART0-RX	Debug UART0 data receive	3.3V	I	
L5	UART1-TX	UART1-TX	UART1 data send	3.3V	O	
L6	UART1-RX	UART1-RX	UART1 data receive	3.3V	I	
L7	UART1-RTS	UART1-RTS	UART1 Data request signal	3.3V	O	
L8	UART1-CTS	UART1-CTS	UART1 Data clearing signal	3.3V	I	
L9	UART2-TX	UART2-TX	UART2 data send	3.3V	O	
L10	UART2-RX	UART2-RX	UART2 data receive	3.3V	I	
L11	BOOT_SEL0	BOOT_SEL0	BOOT configure 0	1.8V	I	
L12	BOOT_SEL1	BOOT_SEL1	BOOT configure 1	1.8V	I	
L13	BOOT_SEL2	BOOT_SEL2	BOOT configure 2	1.8V	I	
L14	BOOT_SEL3	BOOT_SEL3	BOOT configure 3	1.8V	I	
L15	BOOT_SEL4	BOOT_SEL4	BOOT configure 4	1.8V	I	
L16	FEL	FEL	USB burn mirror	1.8V	I	
L17	I2S2_DOUT0	I2S2_DOUT0	I2S2 Data output	3.3V	O	
L18	I2S2_LRCK	I2S2_LRCK	I2S2 Sampling sync signal	3.3V	O	
L19	I2S2_BLCK	I2S2_BLCK	I2S2 Sampling bit clock	3.3V	O	
L20	I2S2_DIN0	I2S2_DIN0	I2S2 Data input	3.3V	I	
L21	I2S2_MLCK	I2S2_MLCK	I2S2 Master clock output	3.3V	O	
L22	SPDIF-OUT	SPDIF-OUT	Digital audio interface	3.3V	O	
L23	LINEOUTR	LINEOUTR	Analog audio output	-	O	
L24	LINEOUTL	LINEOUTL	Analog audio output	-	O	
L25	LINEINR	LINEINR	TBD	-	-	
L26	LINEINL	LINEINL	TBD	-	-	
L27	NC	NC	Reserved unused	-	-	
L28	NC	NC	Reserved unused	-	-	
L29	NC	NC	Reserved unused	-	-	
L30	IR-RX	GPIO	EVK Reference design interrupt input	3.3V	O	
L31	PH8	GPIO	Reserved unused	3.3V	-	
L32	PC2	GPIO	Enable/disable camera	1.8V	O	
L33	PC12	GPIO	Reset Camera	1.8V	O	
L34	PD22	GPIO	Enable/disable carrier board VDD_3V3IO	3.3V	O	
L35	PD27	GPIO	LVDS0 Screen touch TP chip selection	3.3V	O	
L36	PD23	GPIO	LVDS1 Screen touch TP chip selection	3.3V	O	
L37	PD25	GPIO	4G module reset	3.3V	O	
L38	PD20	PD20	LVDS1 Touch TP enabled screen	3.3V	O	
L39	PC7	PC7	MIPI CSI enabled	1.8V	O	
L40	PH9	PH9	HD-LVDS power enabled	3.3V	O	
L41	PD24	PD24	LVDS0 Touch TP enabled screen	3.3V	O	
L42	PD28	PD28	LVDS0 Backlight enabled	3.3V	O	

L43	PWM5	PWM5	HD LVDS Backlight Adjust	3.3V	O	
L44	PD26	PD26	GPIO	3.3V	O	
L45	PD21	PD21	GPIO	3.3V	O	
L46	NC	NC	Reserved unused	-	-	
L47	GPADC3	GPADC3	General ADC channel 3	0~1.8V	I	
L48	GPADC2	GPADC2	General ADC channel 2	0~1.8V	I	
L49	GPADC1	GPADC1	General ADC channel 1	0~1.8V	I	
L50	GPADC0	GPADC0	General ADC channel 0	0~1.8V	I	
L51	LRADC0	LRADC0	Low resolution low speed sampling ADC	0~1.35V	I	
L52	TWI3-SCK	TWI3-SCK	TWI3 clock	3.3V	O	
L53	TWI3-SDA	TWI3-SDA	TWI3 data	3.3V	I/O	
L54	TWI4-SCK	TWI4-SCK	TWI4 clock	3.3V	O	
L55	TWI4-SDA	TWI4-SDA	TWI4 data	3.3V	I/O	
L56	WREQIN	NC	Reserved unused	-	-	
L57	USB2-EXT-IRQ	USB2-EXT-IRQ	USB2 Wake up interrupt	3.3V	I	
L58	DCXO-RFCLK	NC	Reserved unused	-	-	

Table 3-1 MYC-YT507H Core board PIN LIST

4. Electrical Characteristics

4.1. System Power

In order to ensure the normal operation of the core board, the recommended input voltage of the core board is 5V±5% and the current is 2A. The on board model of the core board is AXP853T PMIC power management chip, which generates multiple different voltages by PMIC to meet the power supply of CPU,DDR,EMMC, etc.

Name	Description	Recommended Voltage
VDD_5V	5V input, main supply voltage	5V±5%
VSOM-3V3	External output 3.3V,1A.	
VCC-USB2-3V3	The default output is 3.3V Peripherals mounted on the USB2.Support peripherals to wake up CPU.	

Table 4-1 External power supply voltage

T507-H CPU provides numerous GPIO, these GPIO are grouped so that each group of GPIO can be configured with 3.3V or 1.8V. Users using THE GPIO of MYC-YT507H should be careful that the GPIO level shall not exceed the supply voltage.

PMIC DCDC1,ALDO5,DCDC6 can be configured to output different voltages in the driver code in order to select the power domain of the GPIO group. For inexperienced users, Mill recommends not reconfigure the GPIO voltage for each group as much as possible. If necessary, you can reconfigure the GPIO-PE and GPIO-PI voltages, but make sure they are at the same level as peripherals.

Name	Description	Function	Voltage
GPIO-PA	3.3V	RMII	DCDC1
GPIO-PC	1.8V	eMMC	ALDO1
GPIO-PD	3.3V	LVDS	DCDC1
GPIO-PE	3.3V	DVP CSI	ALDO5 (Support separate voltage adjustment)
GPIO-PF	3.3V	SDIO0	DCDC1
GPIO-PG	3.3V	SDIO1	DCDC1
GPIO-PH	3.3V	UART0/5 IO	DCDC1
GPIO-PI	3.3V	RGMII	DCDC6 (Support separate voltage adjustment)
GPIO-PL	1.8V	VCC-RTC	RTC-LDO

Table 4-2 T507-H GPIO voltages

4.2. Power Consumption

Conditon	Voltage(V)	Average Current (mA)	Power Consumption (W)
During boot	4.97	200	0.994
Full-load stage	4.97	400	1.998
Mem low-power mode	4.97	1	0.005
Freeze Low-power mode	4.97	9	0.045

Table 4-3 Power consumption parameters

4.3. GPIO DC Parameters

Parameter	Symbol	Min	Typical	Max	Units	remark
High-lever DC input voltage	V_{IH}	0.7*VCC_{IO}	—	VCC_{IO}+0.3	V	—
Low-lever DC input voltage	V_{IL}	-0.3	—	0.3*VCC_{IO}	V	—
High-lever DC output voltage	V_{OH}	VCC_{IO}-0.3		VCC_{IO}	V	—
Low-lever DC output voltage	V_{OL}	0	—	0.2	V	—

Table 4-4 GPIO DC Parameters

5. System Start-up Configuration

5.1. Boot Mode

T507-H processors start up by executing programs in the chip's internal BROM. BROM starts by reading BOOT_SEL[4:0] pins into different boot sources. BOOT_SEL pins do not add pull-up or pull-down designs within the core board, but the chip has 15K pull-up designs by default.

BOOT_SEL[4:0] Pin configuration corresponds to the starting device as follows:

BOOT_SEL Pin [4:0]	function	Description
11011	Micro SD->eMMC	Preferentially boot from micro SD card, If no boot image is found, start from eMMC.
10111	Micro SD	The micro SD card is started

Table 5-1 BOOT mode configuration

5.2. Special Function Pin

The MYC-YT507H core board provides three dedicated pins, namely Reset and ONOFF and FEL. Table 5-2 describes the functions and usage of these functions.

function	Description
CPU-RESET	Used to reset the core board. The low level is valid.
CPU-ONOFF	Used to control core board sleep wake up, long press sleep, short press wake up.
FEL	FEL is low when the core board is powered on, and the core board can enter USB download mode to update the program of the core board.

Table 5-2 Special pin function description

6. Interfaces

6.1. SMHC

MYC-YT507H core board leads to two SMHC interfaces, SMHC0 and SMHC1. SMHC0 is commonly used to design micro SD card signals, and SMHC1 can be used to design communication interfaces between modules with SDIO interfaces.

6.1.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
90	SDIO0-D2	SDIO0-D2	SDIO0 data 2	3.3V	I/O	
91	SDIO0-CMD	SDIO0-CMD	SDIO0 command	3.3V	O	
92	SDIO0-D1	SDIO0-D1	SDIO0 data 1	3.3V	I/O	
93	SDIO0-CLK	SDIO0-CLK	SDIO0 clock	3.3V	O	
96	SDIO0-D3	SDIO0-D3	SDIO0 data 3	3.3V	I/O	
97	SDIO0-D0	SDIO0-D0	SDIO0 data 0	3.3V	I/O	
102	SDIO0-DET	SDIO0-DET	SDIO0 card Plug detection	3.3V	I	

Table 6-1 SMHC0 pin description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
94	SDIO1-D3	SDIO1-D3	SDIO1 data 3	3.3V	I/O	
95	SDIO1-D1	SDIO1-D1	SDIO1 data 1	3.3V	I/O	
98	SDIO1-CLK	SDIO1-CLK	SDIO1 clock	3.3V	O	
99	SDIO1-D2	SDIO1-D2	SDIO1 data 2	3.3V	I/O	
100	SDIO1-CMD	SDIO1-CMD	SDIO1 command	3.3V	O	
101	SDIO1-D0	SDIO1-D0	SDIO1 data 0	3.3V	I/O	

Table 6-2 SMHC1 pin description

6.2. UART

MYC-YT507H core board has up to 6 serial ports. Due to the pin reuse of the chip, the core board is configured with 4 serial ports by default, among which UART1 has flow control (RTS and CTS signal) function.

6.2.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L1	UART5-TX	UART5-TX	UART5 data send	3.3V	O	
L2	UART5-RX	UART5-RX	UART5 data receive	3.3V	I	
L3	UART0-TX	UART0-TX	Debug UART0 data send	3.3V	O	
L4	UART0-RX	UART0-RX	Debug UART0 data receive	3.3V	I	
L5	UART1-TX	UART1-TX	UART1 data send	3.3V	O	
L6	UART1-RX	UART1-RX	UART1 data receive	3.3V	I	
L7	UART1-RTS	UART1-RTS	UART1 Data request signal	3.3V	O	
L8	UART1-CTS	UART1-CTS	UART1 Data clear signal	3.3V	I	
L9	UART2-TX	UART2-TX	UART2 data send	3.3V	O	
L10	UART2-RX	UART2-RX	UART2 data receive	3.3V	I	

Table 6-3 UART PIN description

6.3. USB

T507-H chip integrates USB2.0 Host controller and USB2.0 OTG controller. The Host controller can provide three USB2.0 Host interfaces, and the OTG controller provides one USB2.0 interface. MYC-YT507H core board brings it all out. Note that the USB2.0 Host interface cannot be used for the OTG interface.

6.3.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
142	USB0-DN	USB0-DN	USB0 Differential signal -	-	I/O	OTG interface
143	USB0-DP	USB0-DP	USB0 Differential signal +	-	I/O	
145	USB1-DN	USB1-DN	USB1 Differential signal -	-	I/O	USB1 Host
146	USB1-DP	USB1-DP	USB1 Differential signal +	-	I/O	
148	USB2-DN	USB2-DN	USB2 Differential signal -	-	I/O	USB2 Host
149	USB2-DP	USB2-DP	USB2 Differential signal +	-	I/O	
151	USB3-DN	USB3-DN	USB3 Differential signal -	-	I/O	USB3 Host
152	USB3-DP	USB3-DP	USB3 Differential signal +	-	I/O	

Table 6-4 USB PIN description

6.4. Ethernet

The MYC-YT507H core board provides two Ethernet MAC controllers. Contains one RMII interface and one RGMII interface (supporting RMII). Ethernet interface design requires proper network PHY chip.

6.4.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
67	RGMII-MDC	RGMII-MDC	RGMII Manage Data Clock	3.3V	O	When design your carrier board, phy chip support RGMII interface is suitable.
68	RGMII-RXD1	RGMII-RXD1	RGMII Data Receive 1	3.3V	I	
69	GPHY_RST	GPHY_RST	PHY chip reset	3.3V	O	
70	RGMII-RXCTL	RGMII-RXCTL	RGMII Data Receive effective	3.3V	I	
71	RGMII-RXD2	RGMII-RXD2	RGMII Data Receive 2	3.3V	I	
72	RGMII-RXD0	RGMII-RXD0	RGMII Data Receive 0	3.3V	I	
74	RGMII-CLKIN-125M	RGMII-CLKIN-125M	RGMII MAC Parameter clock	3.3V	I	
76	RGMII-RXD3	RGMII-RXD3	RGMII Data Receive 3	3.3V	I	
77	RGMII-RXCK	RGMII-RXCK	RGMII Receive clock	3.3V	I	
78	RGMII-MDIO	RGMII-MDIO	RGMII Manage Data	3.3V	I/O	
79	GPHY-CLK-25M	GPHY-CLK-25M	25Mhz clock output	3.3V	O	
80	RGMII-TXD1	RGMII-TXD1	RGMII data send 1	3.3V	O	
81	RGMII-TXD3	RGMII-TXD3	RGMII data send 3	3.3V	O	
82	RGMII-TXCTL	RGMII-TXCTL	RGMII Send control	3.3V	O	
85	RGMII-TXCK	RGMII-TXCK	RGMII Send clock	3.3V	O	
87	RGMII-TXD0	RGMII-TXD0	RGMII data send 0	3.3V	O	
88	RGMII-TXD2	RGMII-TXD2	RGMII data send 2	3.3V	O	
154	RMII-TXEN	RMII-TXEN	RMII send enable	3.3V	O	
155	RMII-TXCK	RMII-TXCK	RMII Send clock	3.3V	O	When design your carrier board, phy chip support RMII interface is suitable.
156	RMII-RXD1	RMII-RXD1	RMII Data Receive 1	3.3V	I	
157	RMII-CRS-RXDV	RMII-CRS-RXDV	RMII Carrier sense received data enable	3.3V	I	
158	RMII-RXD0	RMII-RXD0	RMII Data Receive 0	3.3V	I	
159	RMII-RXER	RMII-RXER	RMII Receive error	3.3V	I	
160	RMII-MDIO	RMII-MDIO	RMII Manage Data	3.3V	I/O	
161	RMII-MDC	RMII-MDC	RMII Manage clock	3.3V	O	
162	RMII-TXD0	RMII-TXD0	RMII data send 0	3.3V	O	
163	RMII-TXD1	RMII-TXD1	RMII data send 1	3.3V	O	
164	EPHY_RST	EPHY_RST	PHY chip reset	3.3V	O	

Table 6-5 Ethernet pin description

6.5. MIPI CSI

MYC-YT507H provides a 4-lane MIPI CSI camera input interface. MIPI CSI interface supports 8M@30fps or 1080p@25fps.

6.5.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
104	MCSI-MCLK	MCSI-MCLK	MIPI CSI Base clock output	-	I	
105	MCSI-SDA	MCSI-SDA	MIPI CSI I2C Data	-	I	
106	MCSI-SCK	MCSI-SCK	MIPI CSI I2C clock	-	I	
108	MCSI-CLKP	MCSI-CLKP	MIPI CSI differential clock+	-	I	
109	MCSI-CLKN	MCSI-CLKN	MIPI CSI differential clock-	-	I	
111	MCSI-D0P	MCSI-D0P	MIPI CSI differential data 0+	-	I	
112	MCSI-D0N	MCSI-D0N	MIPI CSI differential data 0-	-	I	
114	MCSI-D1P	MCSI-D1P	MIPI CSI differential data 1+	-	I	
115	MCSI-D1N	MCSI-D1N	MIPI CSI differential data 1-	-	I	
117	MCSI-D2P	MCSI-D2P	MIPI CSI differential data 2+	-	I	
118	MCSI-D2N	MCSI-D2N	MIPI CSI differential data 2-	-	I	
120	MCSI-D3P	MCSI-D3P	MIPI CSI differential data 3+	-	I	
121	MCSI-D3N	MCSI-D3N	MIPI CSI differential data 3-	-	I	

Table 6-6 MIPI CSI PIN description

6.6. Parallel CSI

The Parallel CSI interface of MYC-YT507H core board can support up to 5M@15fps or 1080p@30fps video input signal.

6.6.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
43	NCSI0-SCK	NCSI0-SCK	Parallel CSI I2C clock	3.3V	O	The default voltage of the IO port is set to 3.3V. PMIC can be controlled through the TWI port to adjust the VOLTAGE of the IO port, such as 1.8V/2.8V
44	NCSI0-SDA	NCSI0-SDA	Parallel CSI I2C data	3.3V	I/O	
45	NCSI0-HSYNC	NCSI0-HSYNC	Parallel CSI Line sync signal	3.3V	I	
46	NCSI0-D7	NCSI0-D7	Parallel CSI data 7	3.3V	I	
47	NCSI0-PCLK	NCSI0-PCLK	Parallel CSI input pixel clock	3.3V	I	
48	NCSI0-D6	NCSI0-D6	Parallel CSI data 6	3.3V	I	
49	NCSI0-D5	NCSI0-D5	Parallel CSI data 5	3.3V	I	
50	NCSI0-D3	NCSI0-D3	Parallel CSI data 3	3.3V	I	
51	NCSI0-D2	NCSI0-D2	Parallel CSI data 2	3.3V	I	
52	NCSI0-D4	NCSI0-D4	Parallel CSI data 4	3.3V	I	
53	NCSI0-D0	NCSI0-D0	Parallel CSI data 0	3.3V	I	
54	NCSI0-D1	NCSI0-D1	Parallel CSI data 1	3.3V	I	
55	NCSI0-VSYNC	NCSI0-VSYNC	Parallel CSI field sync signal	3.3V	I	
56	NCSI0-D15	NCSI0-D15	Parallel CSI data 15	3.3V	I	
57	CSI-FSIN0	CSI-FSIN0	Reserved unused	3.3V	I	
58	NCSI0-D14	NCSI0-D14	Parallel CSI data 14	3.3V	I	
59	NCSI0-D13	NCSI0-D13	Parallel CSI data 13	3.3V	I	
60	NCSI0-MCLK	NCSI0-MCLK	Parallel CSI output clock	3.3V	O	
61	NCSI0-D12	NCSI0-D12	Parallel CSI data 12	3.3V	I	
62	NCSI0-D11	NCSI0-D11	Parallel CSI data 11	3.3V	I	
63	NCSI0-D10	NCSI0-D10	Parallel CSI data 10	3.3V	I	
64	NCSI0-D9	NCSI0-D9	Parallel CSI data 9	3.3V	I	
65	NCSI0-D8	NCSI0-D8	Parallel CSI data 8	3.3V	I	

Table 6-7 Parallel CSI PIN description

6.7. LVDS

MYC-YT507H core board supports LVDS signal output. MYC-YT507H provides two Single Link LVDS interfaces to support 1366x768@60fps display output. In addition, two Single Link LVDS can form Dual Link LVDS to support higher display resolution 1920x1080@60fps.

6.7.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
13	LVDS1-D1N	LVDS1-D1N	LVDS1 differential data 1-	3.3V	O	1. LVDS1,LVDS0 can be configured as two independent display interfaces with a resolution of 1366x768@60fps 2. LVDS0, LVDS1 can be configured as HD (dual channel) LVDS with reachable resolution 1920x1080@60fps 3. The core board is configured with LVDS function by default.
14	LVDS1-D1P	LVDS1-D1P	LVDS1 differential data 1+	3.3V	O	
16	LVDS1-D3N	LVDS1-D3N	LVDS1 differential data 3-	3.3V	O	
17	LVDS1-D3P	LVDS1-D3P	LVDS1 differential data 3+	3.3V	O	
19	LVDS1-D2N	LVDS1-D2N	LVDS1 differential data 2-	3.3V	O	
20	LVDS1-D2P	LVDS1-D2P	LVDS1 differential data 2+	3.3V	O	
22	LVDS1-CLKN	LVDS1-CLKN	LVDS1 differential clock -	3.3V	O	
23	LVDS1-CLKP	LVDS1-CLKP	LVDS1 differential clock +	3.3V	O	
25	LVDS1-D0N	LVDS1-D0N	LVDS1 differential data 1-	3.3V	O	
26	LVDS1-D0P	LVDS1-D0P	LVDS1 differential data 1+	3.3V	O	
28	LVDS0-D2N	LVDS0-D2N	LVDS0 differential data 2-	3.3V	O	
29	LVDS0-D2P	LVDS0-D2P	LVDS0 differential data 2+	3.3V	O	
31	LVDS0-D1N	LVDS0-D1N	LVDS0 differential data 1-	3.3V	O	
32	LVDS0-D1P	LVDS0-D1P	LVDS0 differential data 1+	3.3V	O	
34	LVDS0-D0N	LVDS0-D0N	LVDS0 differential data 0-	3.3V	O	
35	LVDS0-D0P	LVDS0-D0P	LVDS0 differential data 0+	3.3V	O	
37	LVDS0-CLKN	LVDS0-CLKN	LVDS0 differential clock -	3.3V	O	
38	LVDS0-CLKP	LVDS0-CLKP	LVDS0 differential clock +	3.3V	O	
40	LVDS0-D3N	LVDS0-D3N	LVDS0 differential data 3-	3.3V	O	
41	LVDS0-D3P	LVDS0-D3P	LVDS0 differential data 3+	3.3V	O	

Table 6-8 LVDS PIN description

6.8. HDMI

MYC-YT507H core board native support one HDMI display output interface, the highest support 4K@60fps resolution.

6.8.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
125	HDMI-CEC	HDMI-CEC	HDMI CEC signal	1.8V	I	
126	HDMI-SDA	HDMI-SDA	HDMI Serial data	1.8V	I/O	
127	HDMI-SCL	HDMI-SCL	HDMI serial clock	1.8V	O	
128	HDMI-HPD	HDMI-HPD	HDMI Hot swap signal	1.8V	I	
130	HTXCP	HTXCP	HDMI TMDS Differential clock signal+	-	O	
131	HTXCN	HTXCN	HDMI TMDS Differential clock signal-	-	O	
133	HTX1P	HTX1P	HDMI TMDS Differential data 1+	-	O	
134	HTX1N	HTX1N	HDMI TMDS Differential data 1-	-	O	
136	HTX0P	HTX0P	HDMI TMDS Differential data 0+	-	O	
137	HTX0N	HTX0N	HDMI TMDS Differential data 0-	-	O	
139	HTX2P	HTX2P	HDMI TMDS Differential data 2+	-	O	
140	HTX2N	HTX2N	HDMI TMDS Differential data 2-	-	O	

Table 6-9 HDMI PIN description

6.9. TV CVBS Output

MYC-YT507H core board supports one TV CVBS Output interface and NTSC and PAL modes.

6.9.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
123	TV-OUT	TV-OUT	Analog video output	0~1.8V	O	

Table 6-10 TV CVBS Output PIN description

6.10. SPDIF-OUT

MYC-YT507H core board supports 1 channel SPDIF OUT digital audio output interface.

6.10.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L22	SPDIF-OUT	SPDIF-OUT	Digital audio interface output	3.3V	O	

Table 6-11 SPDIF-Out PIN description

6.11. I2S

MYC-YT507H core board provides a maximum of three I2S interfaces. Due to pin reuse, one I2S interface is configured by default.

6.11.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L17	I2S2_DOUT0	I2S2_DOUT0	I2S2 Data output	3.3V	O	
L18	I2S2_LRCK	I2S2_LRCK	I2S2 Sampling sync signal	3.3V	O	
L19	I2S2_BLCK	I2S2_BLCK	I2S2 Sampling bit clock	3.3V	O	
L20	I2S2_DIN0	I2S2_DIN0	I2S2 Data input	3.3V	I	
L21	I2S2_MLCK	I2S2_MLCK	I2S2 Master clock output	3.3V	O	

Table 6-12 I2S PIN description

6.12. Line Out

T507-H native supports line Out output. MYC-YT507H core board is directly connected to the line Out interface.

6.12.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L23	LINEOUTR	LINEOUTR	Analog audio output	-	O	
L24	LINEOUTL	LINEOUTL	Analog audio output	-	O	

Table 6-13 Line Out PIN description

6.13. GPIO

Most of the GPIO pins of MYC-YT507H core board are used as specific functional interfaces, and some GPIO pins are still used as GPIO by default.

6.13.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L30	IR-RX	GPIO	EVK Reference design interrupt input	3.3V	O	
L31	PH8	GPIO	Reserved unused	3.3V	-	
L32	PC2	GPIO	Enable/disable camera	1.8V	O	
L33	PC12	GPIO	Reset Camera	1.8V	O	
L34	PD22	GPIO	Enable/disable carrier board VDD_3V3IO	3.3V	O	
L35	PD27	GPIO	LVDS0 Screen touch TP chip selection	3.3V	O	
L36	PD23	GPIO	LVDS1 Screen touch TP chip selection	3.3V	O	
L37	PD25	GPIO	4G module reset	3.3V	O	
L38	PD20	PD20	LVDS1 Touch TP enabled screen	3.3V	O	
L39	PC7	PC7	MIPI CSI enabled	1.8V	O	
L40	PH9	PH9	HD-LVDS power enabled	3.3V	O	
L41	PD24	PD24	LVDS0 Touch TP enabled screen	3.3V	O	
L42	PD28	PD28	LVDS0 Backlight enabled	3.3V	O	
L43	PWM5	PWM5	HD LVDS Backlight Adjust	3.3V	O	
L44	PD26	PD26	GPIO	3.3V	O	
L45	PD21	PD21	GPIO	3.3V	O	

Table 6-14 GPIO PIN description

6.14. ADC

MYC-YT507H core board supports GPADC and LRADC. GPADC has a 12-bit resolution, a maximum sampling rate of 1Mhz, and supports a signal input range of 0~1.8V. LRADC supports a maximum resolution of 6 bits and a sampling rate of 2Khz. The corresponding LRADC supports a range of 0~ 1.35v input signals.

6.14.1. Pin Description

Pin	Signal	Default Function	Description	Voltage	IO	Comments
L47	GPADC3	GPADC3	General ADC channel 3	0~1.8V	I	
L48	GPADC2	GPADC2	General ADC channel 2	0~1.8V	I	
L49	GPADC1	GPADC1	General ADC channel 1	0~1.8V	I	
L50	GPADC0	GPADC0	General ADC channel 0	0~1.8V	I	
L51	LRADC0	LRADC0	Low resolution low speed sampling ADC	0~1.35V	I	

Table 6-15 ADC PIN description

7. Package Information

7.1. Package Dimensions

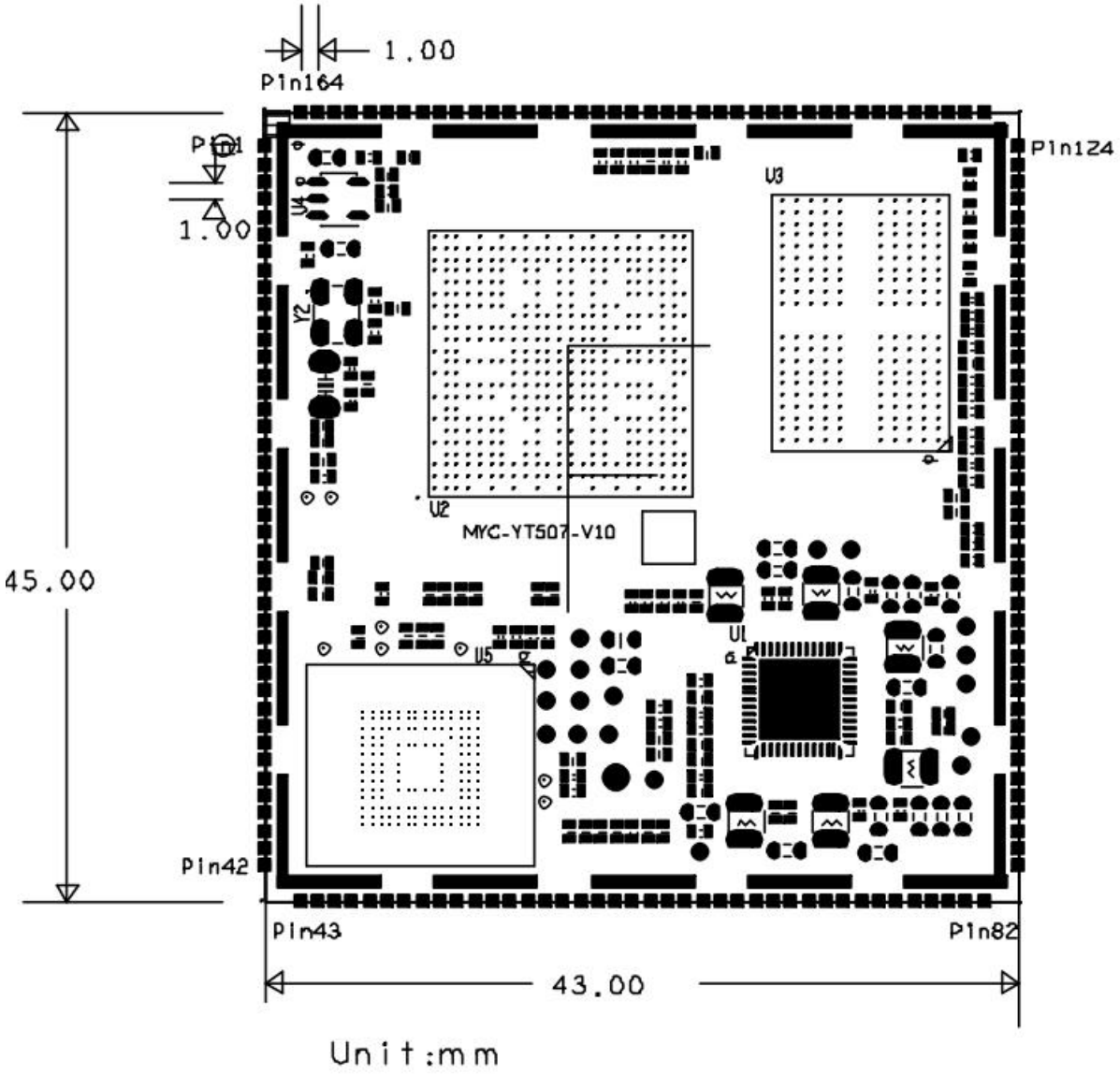

Figure 7-1 MYC-YT507H Core board Bottom view

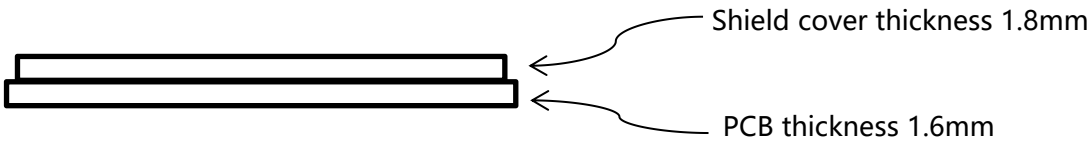

Figure 7-2 MYC-C8MMX-V2 Core board side view

7.2. Carrier Board PCB Requirements

MYC-YT507H Pad design size has 2 kinds of specifications: oval hole and round hole two ways. Figure 7-4 shows the design reference sizes of the two pads respectively.

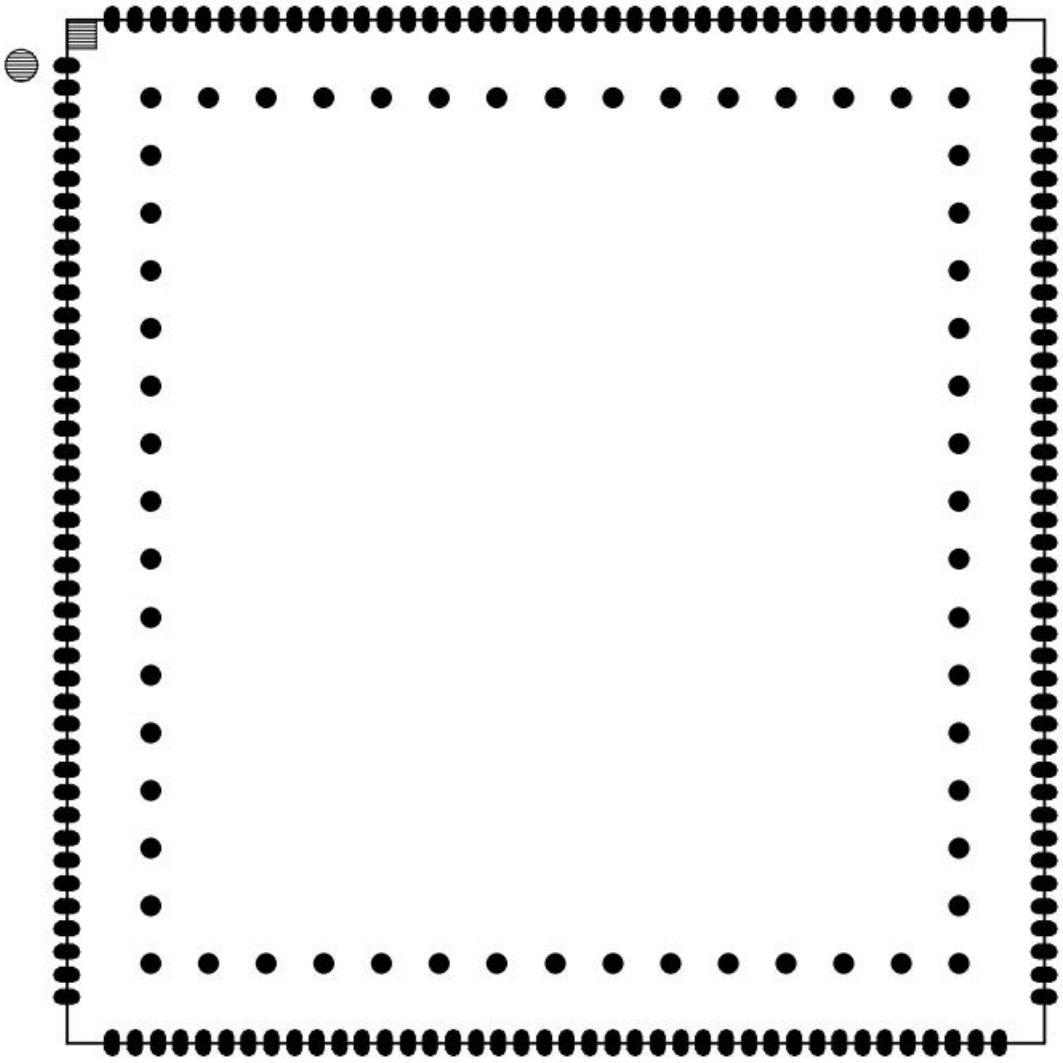

Figure 7-3 MYC-YT507H Core board PCB encapsulation

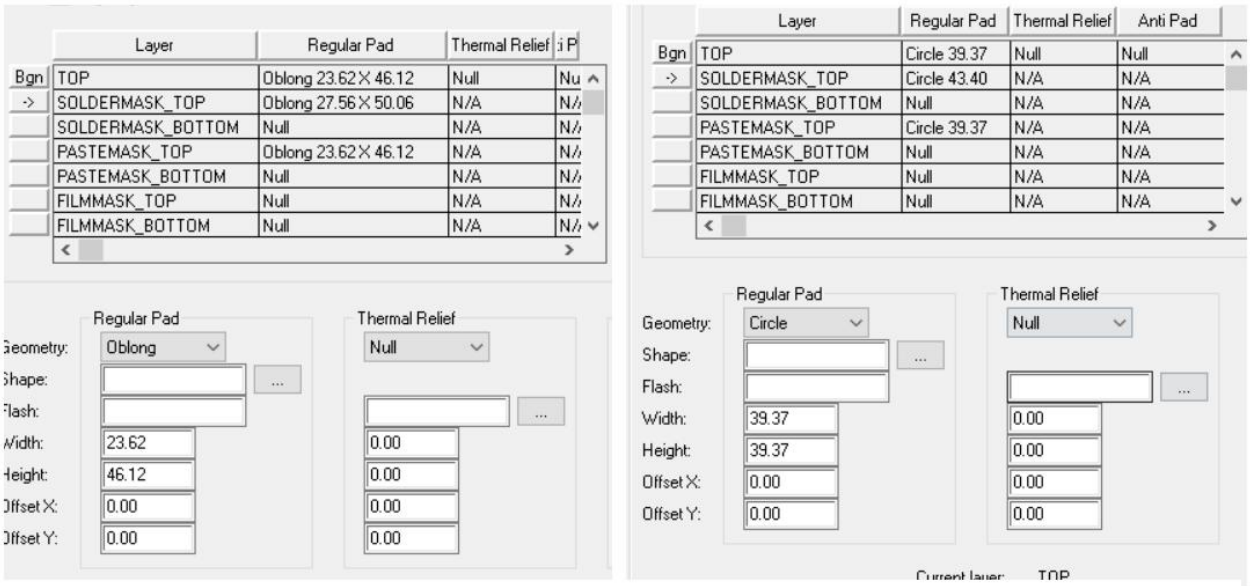

Figure 7-4 MYC-YT507H carrier board PCB Sealing dimensions

MYIR Electronics provides designed PCB packages. Please visit http://d.myirtech.com/MYD-YT507H/ for this information.

7.3. carrier board PCB requirement

A) The thickness of PCB is recommended to be at least 1.6mm, and the balance of copper coating should be paid attention to. If PCB deformation occurs after passing through the furnace, it is recommended to use a carrier to fix passing through the furnace.

B) To ensure the quality of mounting and tin, please ensure that the distance between modules and other components on the PCB is at least 3mm.

C) Please design the package of the core board module according to Section 7.2, or use the PCB package provided by Mill Electronics.

7.4. PCB manufacture technology

A) It is recommended that the circular pad with 0.15mm stencil thickness open the hole ratio 1:1; For 0.18mm thickness, the opening ratio is 1:0.8.

B) PCB stencil requirements for stamp hole pads are recommended for internal retracement of 10%, external expansion of 20%,with thickness of 0.18mm step stencil.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

- To help customers compile and run the source code we offer;
- To help customers solve problems occurred during operations if users follow the user manual documents;
- To judge whether the failure exists;

- To provide free software upgrading service.
- However, the following situations are not included in the scope of our free technical support service:
- Hardware or software problems occurred during customers' own development;
- Problems occurred when customers compile or run the OS which is tailored by themselves;
- Problems occurred during customers' own applications development;
- Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

- The warranty period is expired;
- The customer cannot provide proof-of-purchase or the product has no serial number;
- The customer has not followed the instruction of the manual which has caused the damage the product;
- Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;
- Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;
- Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;
- Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

- MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.
- Please do not use finger nails or hard sharp object to touch the surface of the LCD.
- MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.
- Do not clean the surface of the screen with chemicals.
- Please read through the product user manual before you using MYIR's products.
- For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

- MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.
- MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.
- MYIR provides other products supporting services like power adapter, LCD panel, etc.
- ODM/OEM services.

MYIR Electronics Limited

Room 04, 6th Floor, Building No.2, Fada Road,

Yunli Inteiligent Park, Bantian, Longgang District.

Support Email: support@myirtech.com

Sales Email: sales@myirtech.com

Phone: +86-755-22984836

Fax: +86-755-25532724

Website: www.myirtech.com